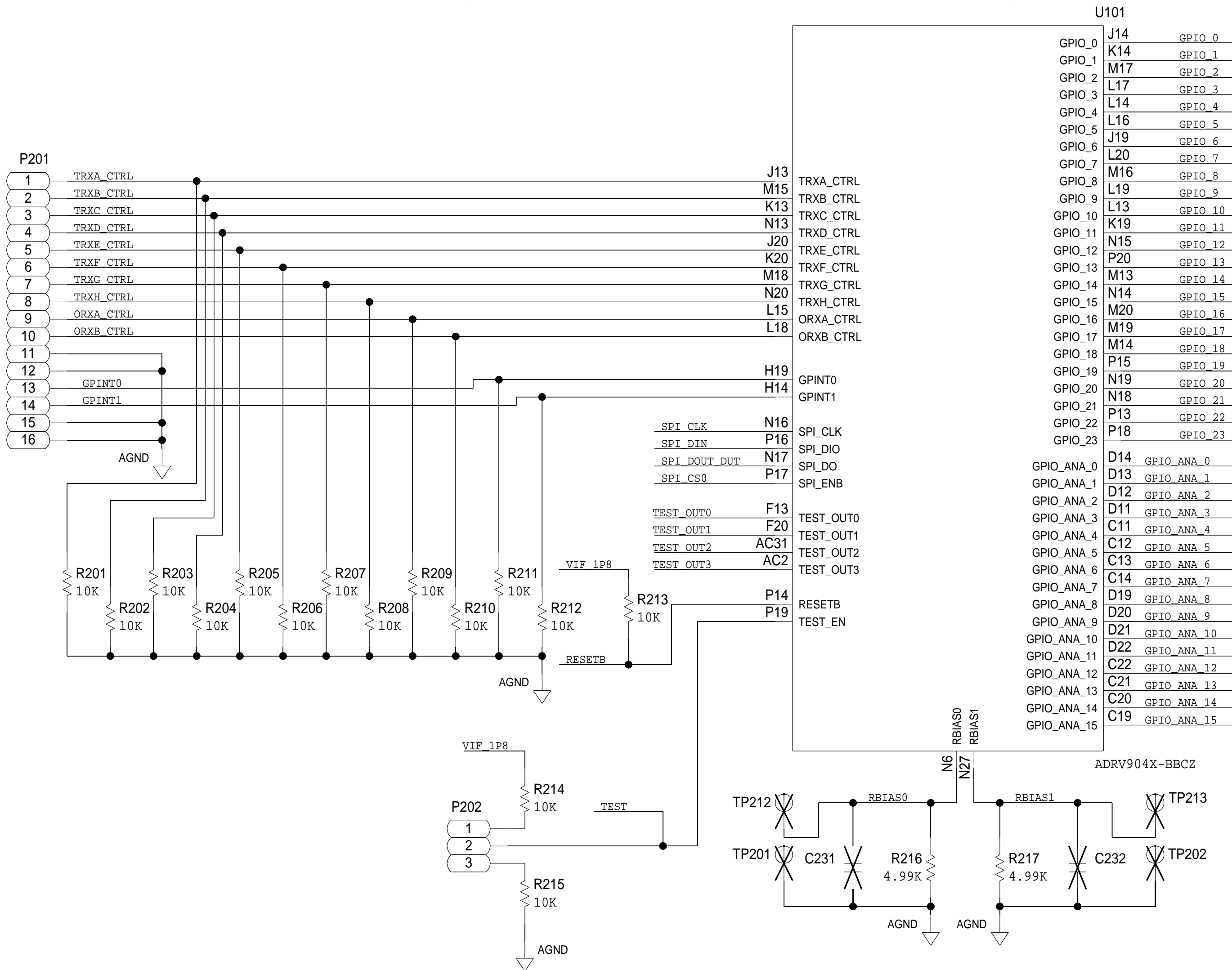
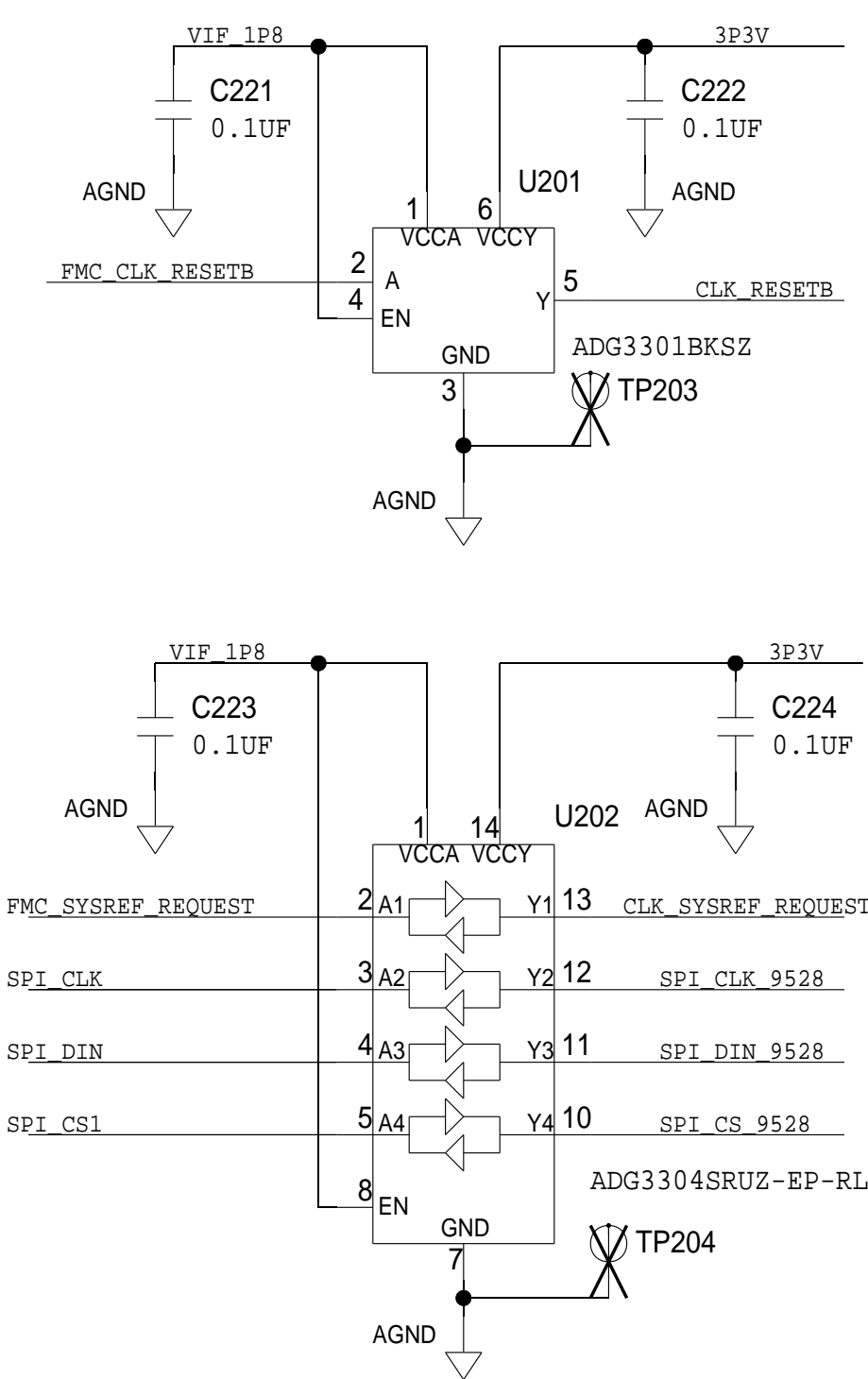


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D	THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.					JUMPER TABLE			REVISIONS																																																																																																																													
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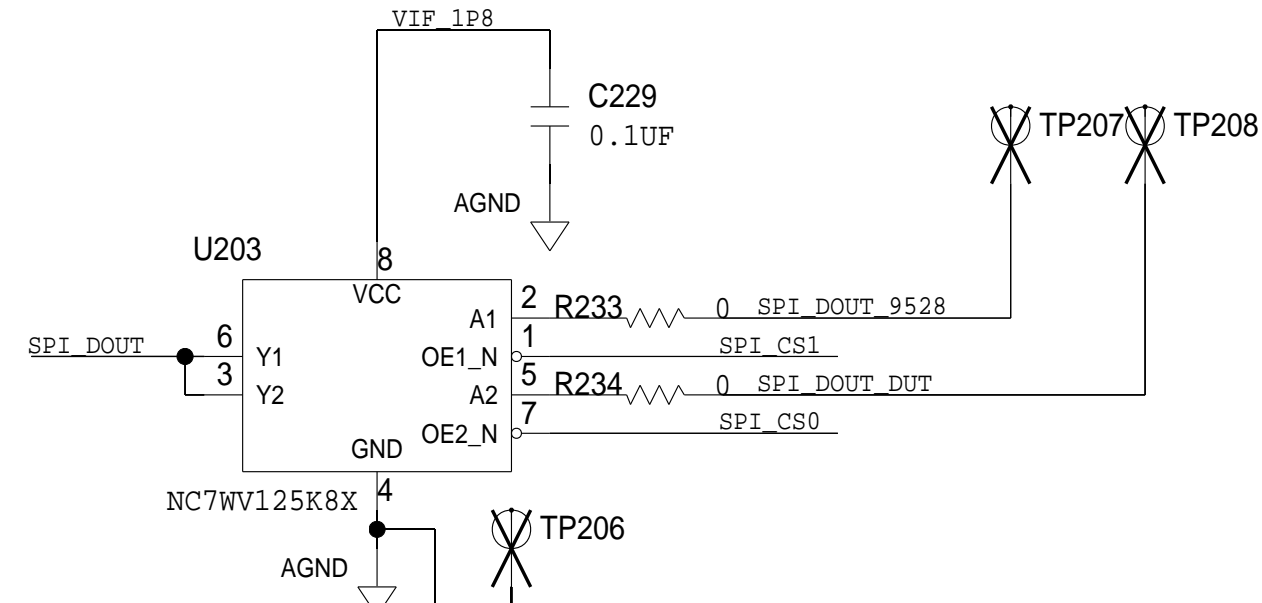
DIGITAL / ANALOG I/O



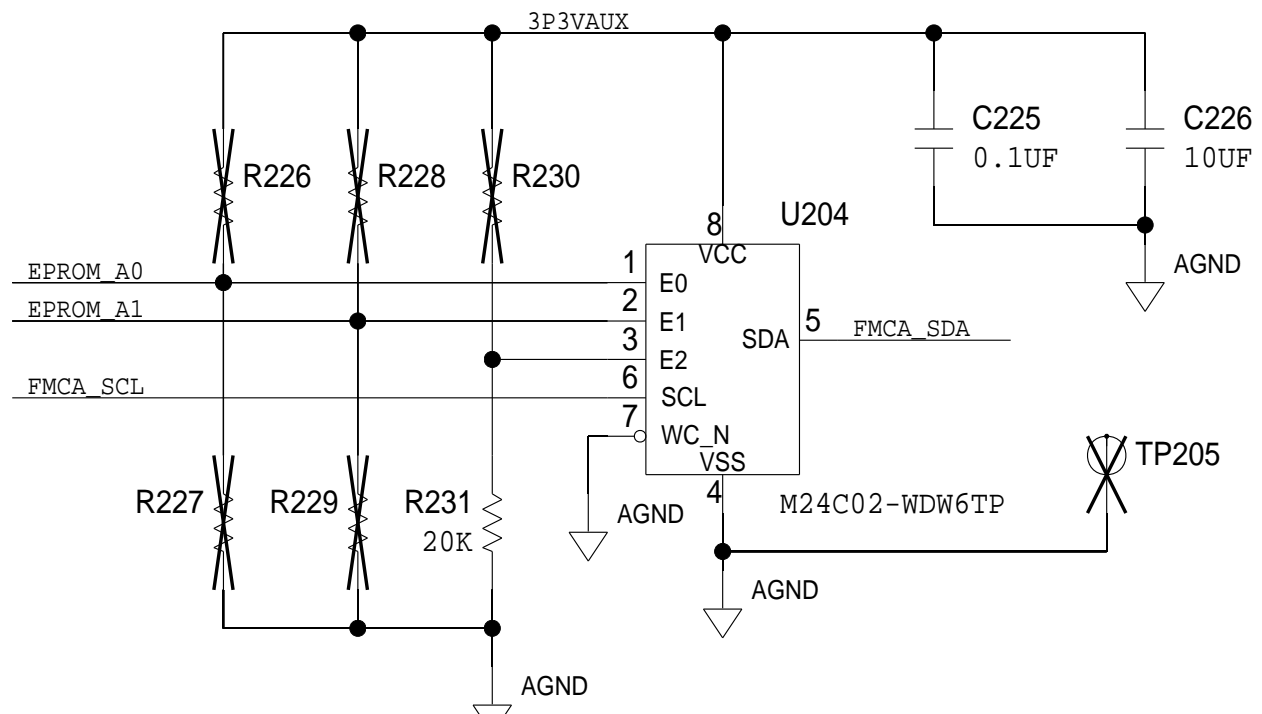
LEVEL SHIFTERS



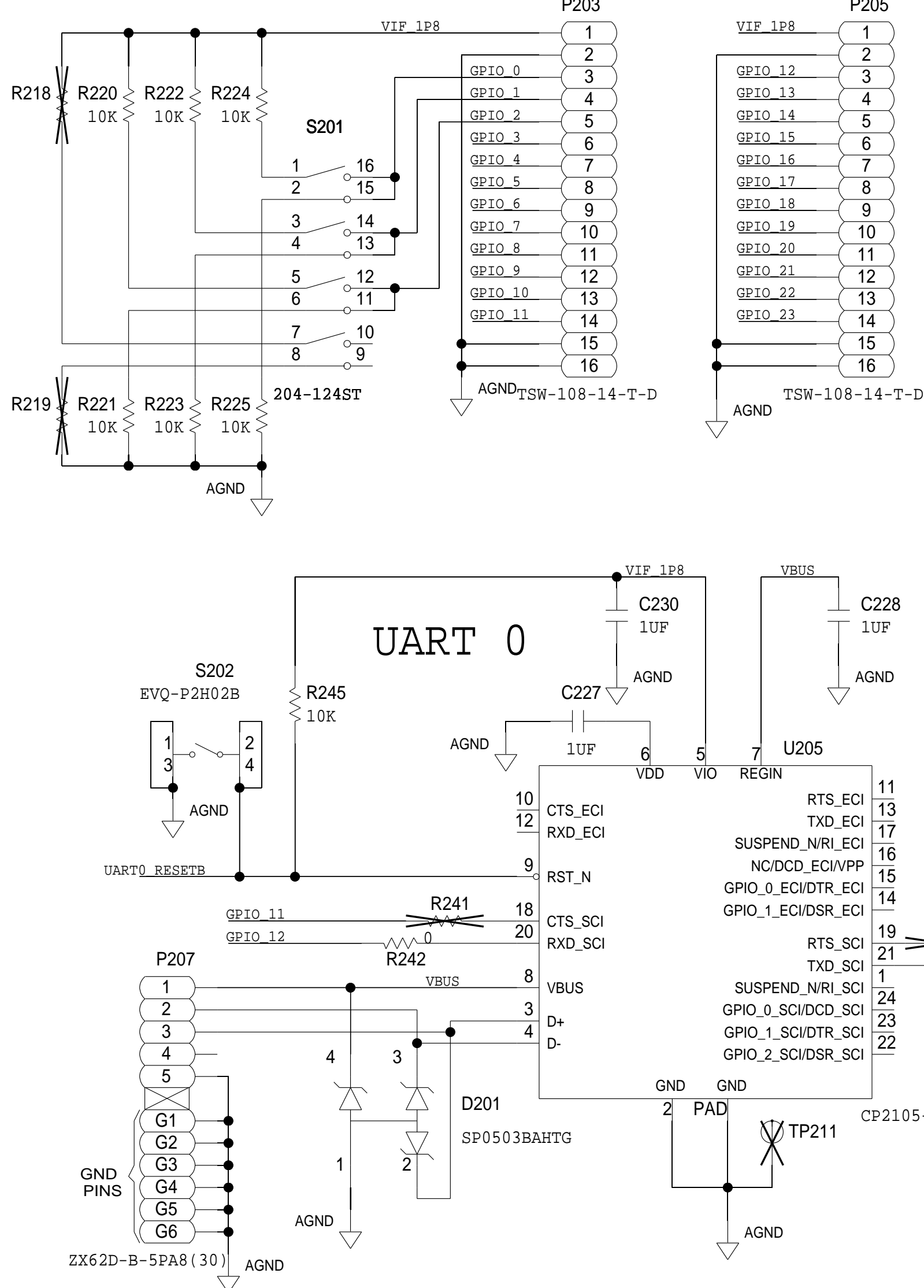
SPI INTERFACE BUFFER



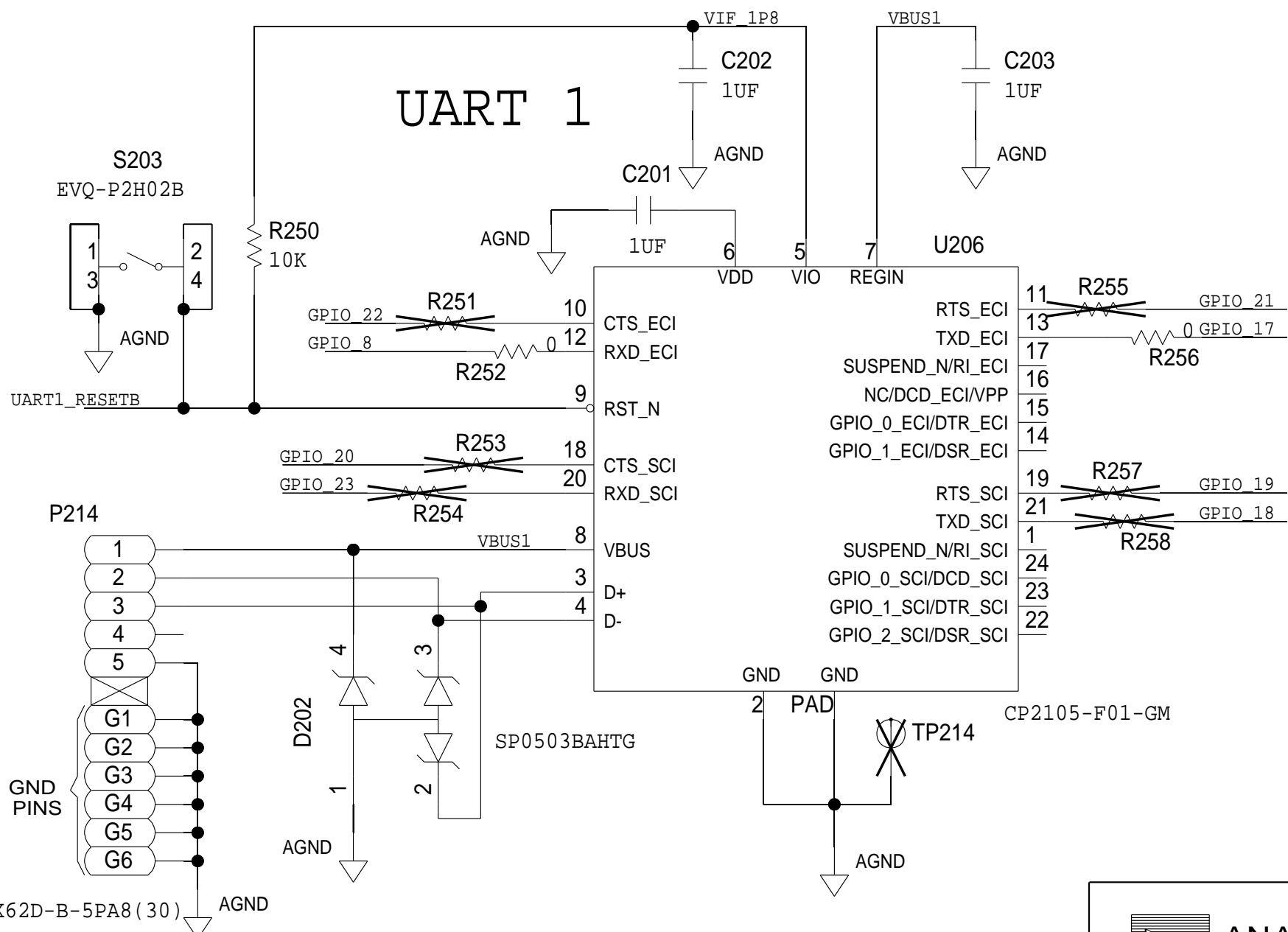
BOARD ID EEPROM



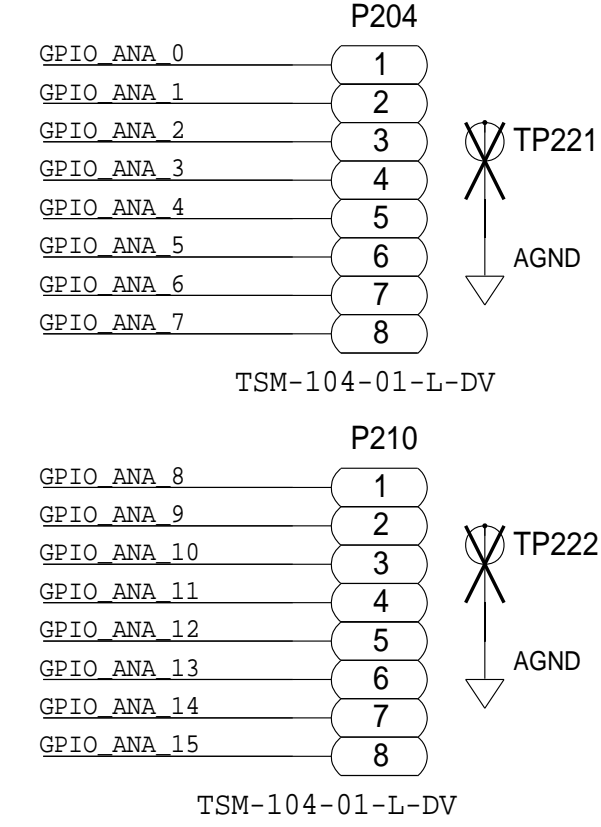
DIGITAL GPIO



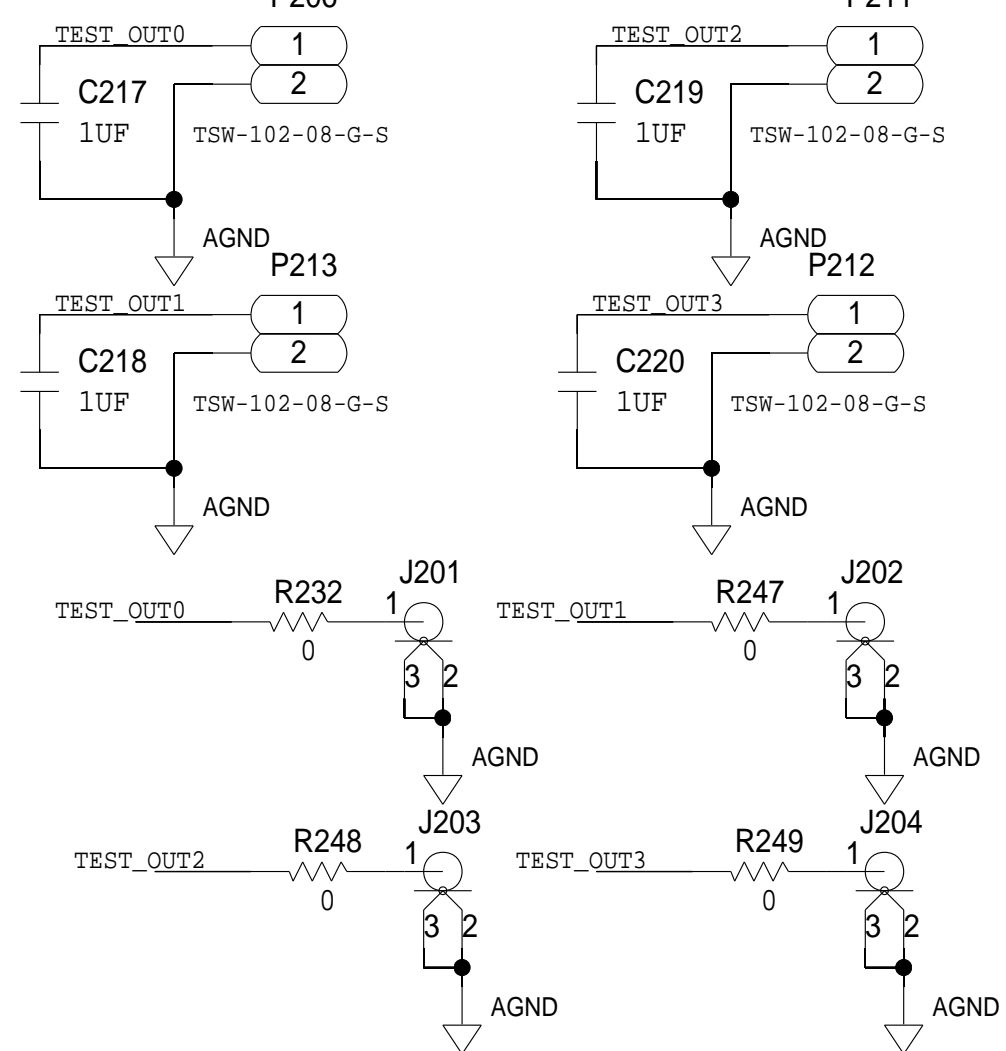
UART 1



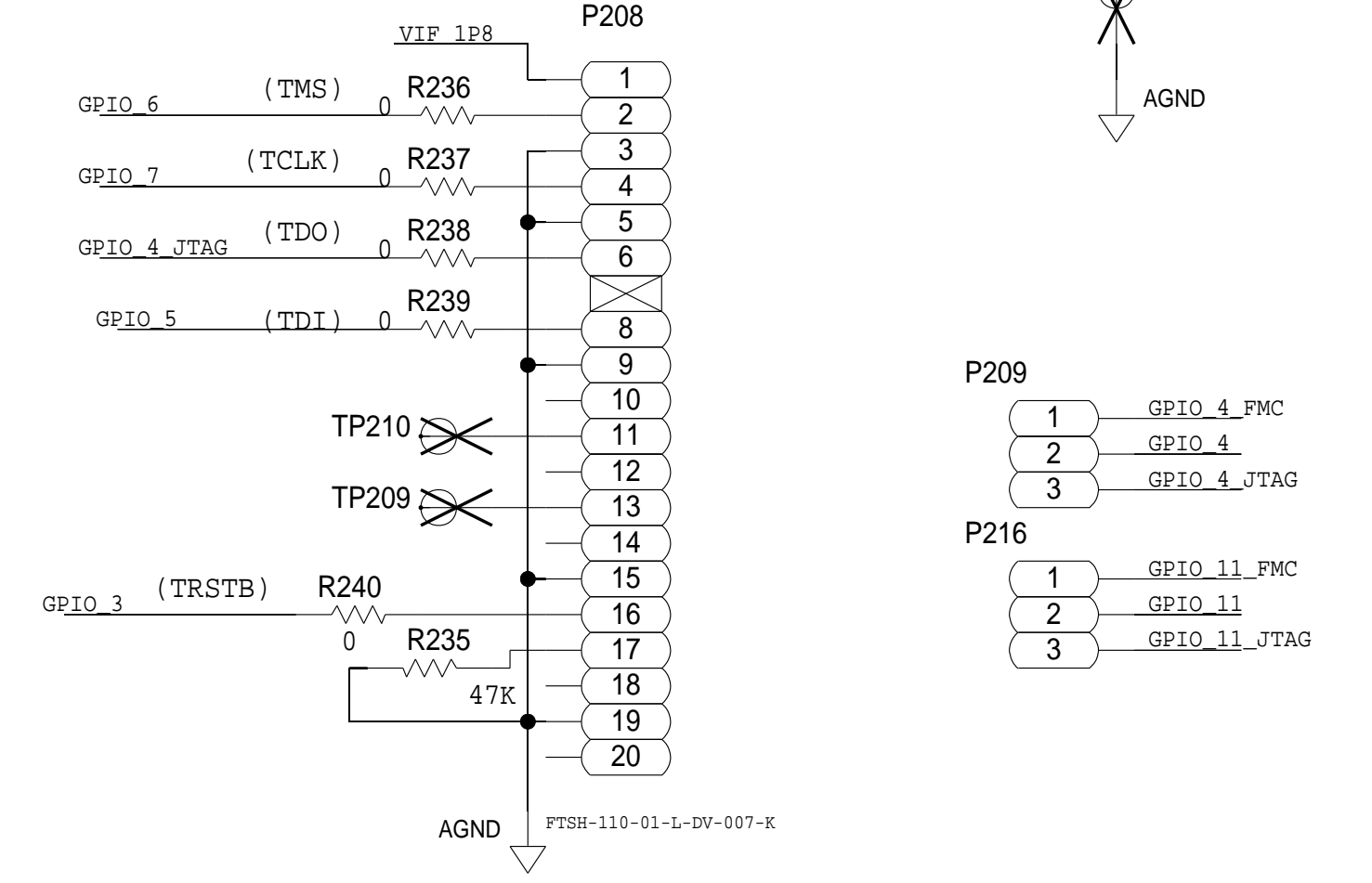
ANALOG GPIC



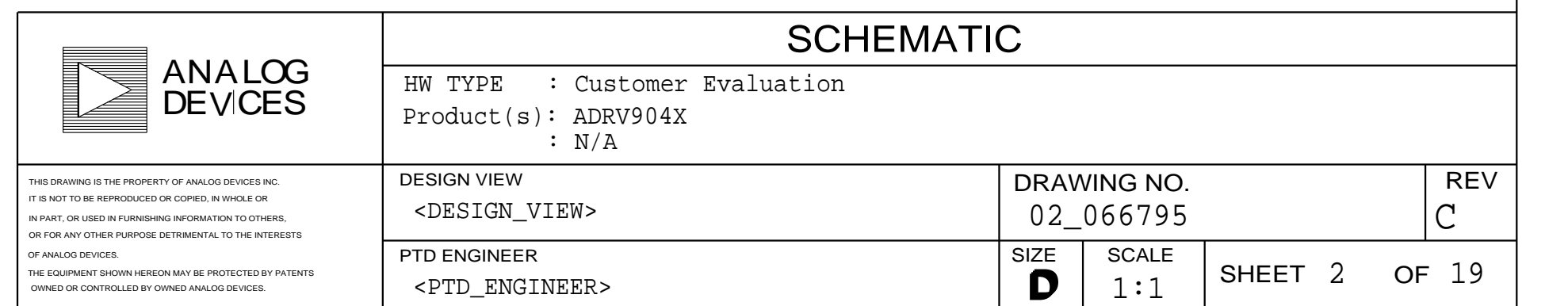
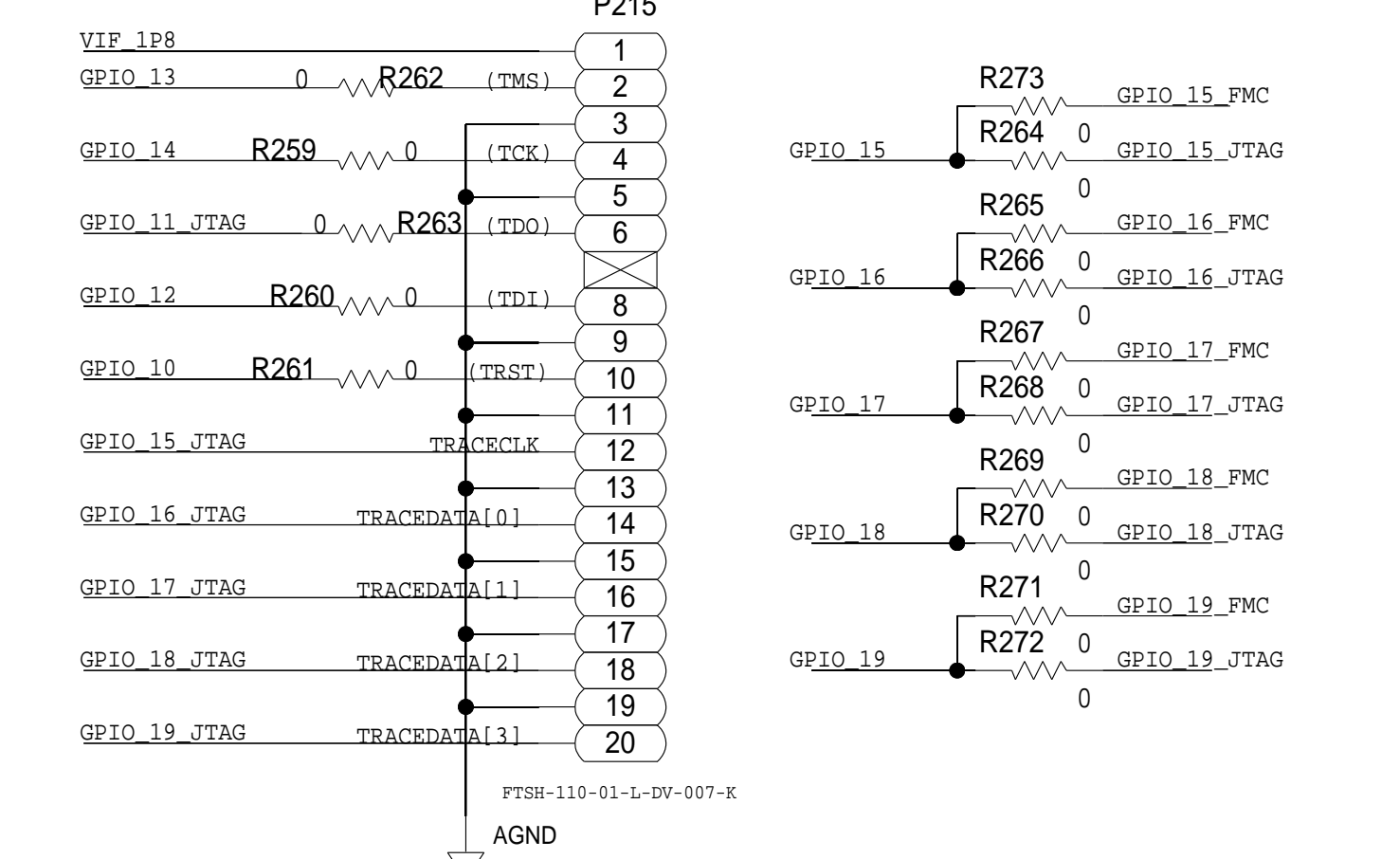
TEST OUT



M4 JTAG INTERFACE



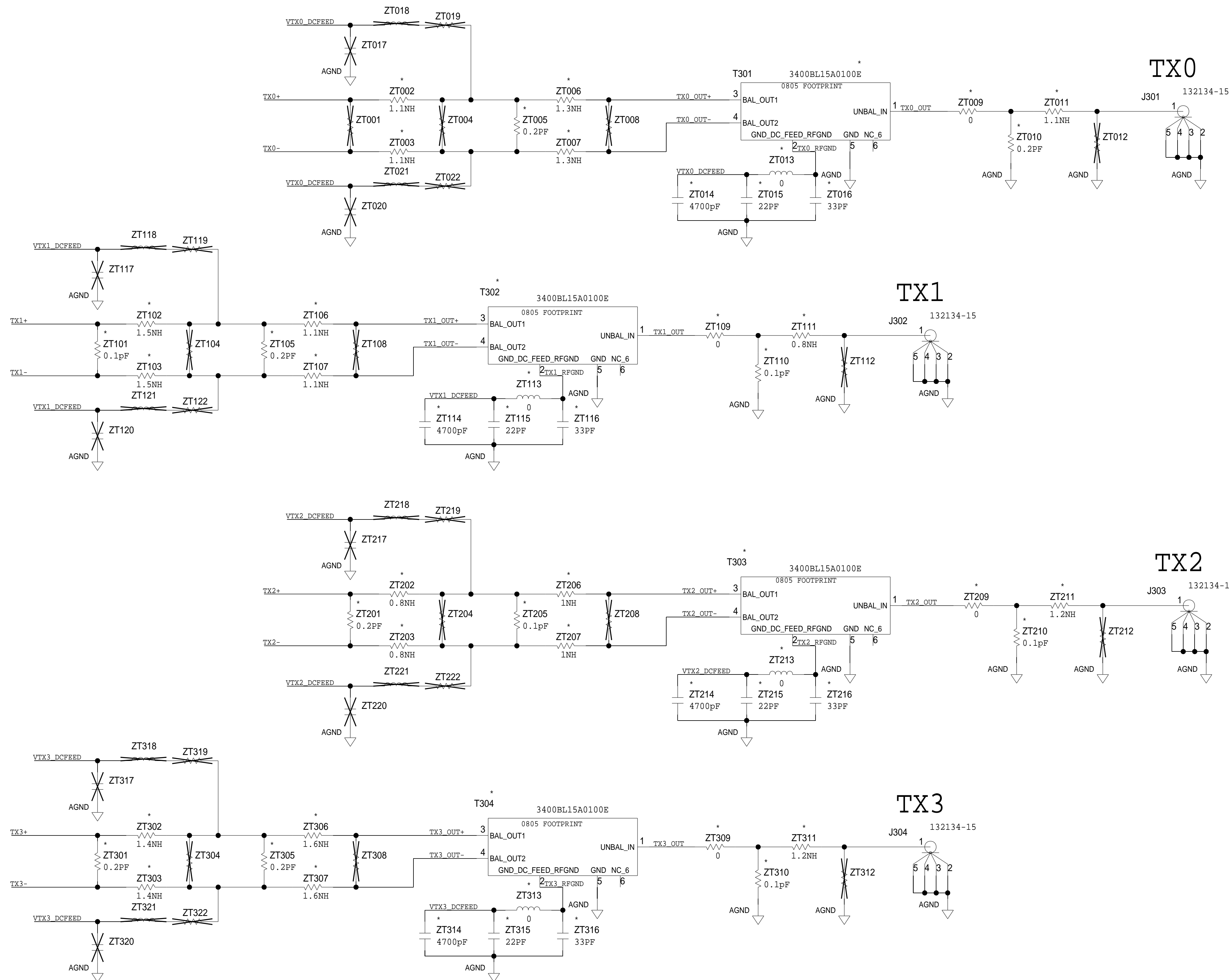
A55 JTAG INTERFACE



TRANSMITTER RF OUTPUT

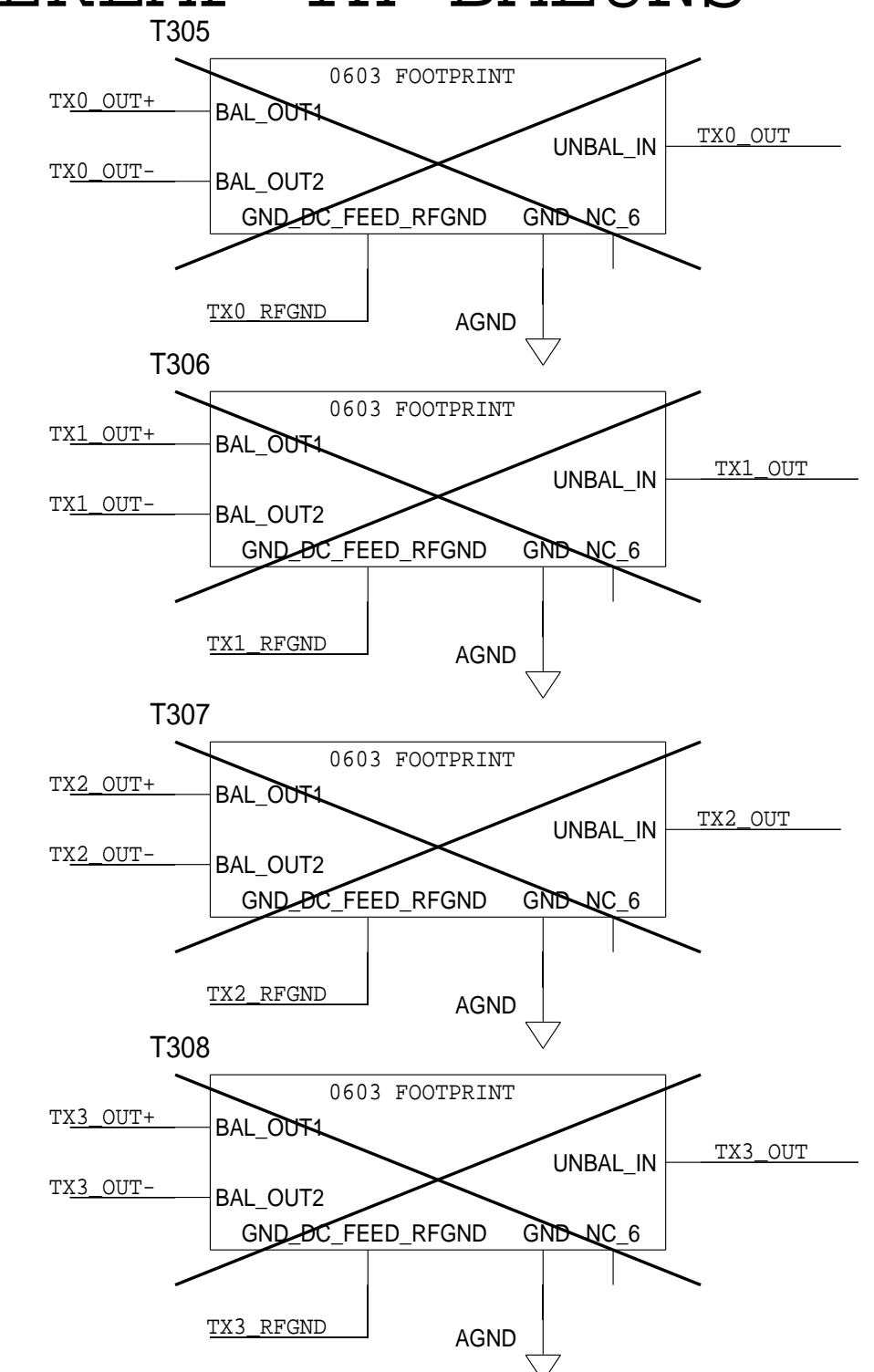
EV6 MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



U101		
	B1	TX0-
TX0N	C1	TX0+
	G1	TX1-
TX1N	H1	TX1+
TX1P	R1	TX2-
TX2N	T1	TX2+
TX2P	Y1	TX3-
TX3N	AA1	TX3+
TX3P	C32	TX4-
TX4N	B32	TX4+
TX4P	H32	TX5-
TX5N	G32	TX5+
TX5P	T32	TX6-
TX6N	R32	TX6+
TX6P	AA32	TX7-
TX7N	Y32	TX7+
TX7P		

OVERLAP TX BALUNS

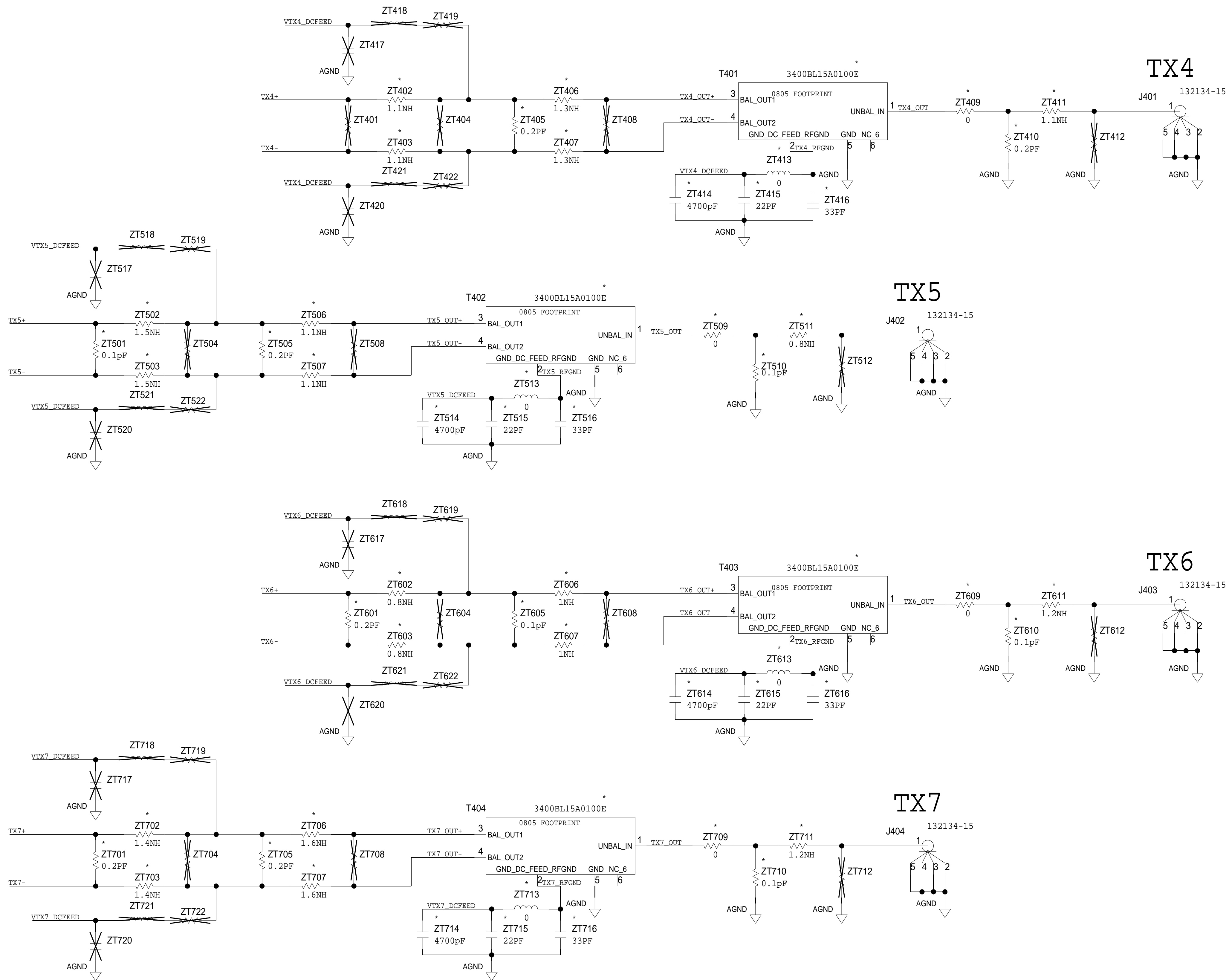


 ANALOG DEVICES	<h2 style="text-align: center;">SCHEMATIC</h2>				
	HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A				
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART - OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETERMINATE, TO THE INTERESTS OF ANALOG DEVICES.</small>	DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_066795		REV C
	PTD ENGINEER <PTD_ENGINEER>		SIZE D	SCALE 1:1	SHEET 3 OF 19

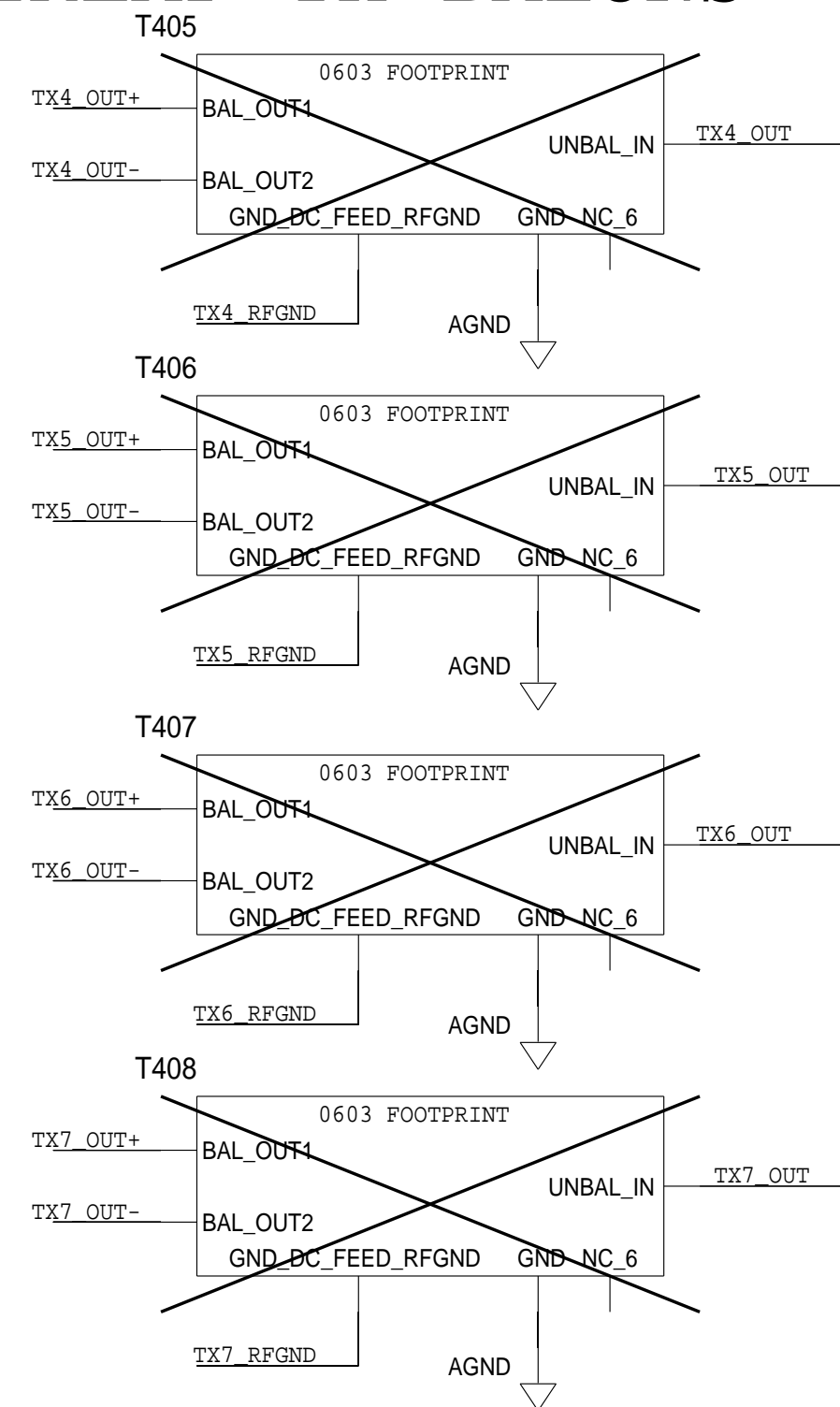
TRANSMITTER RF OUTPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



OVERLAP TX BALUNS

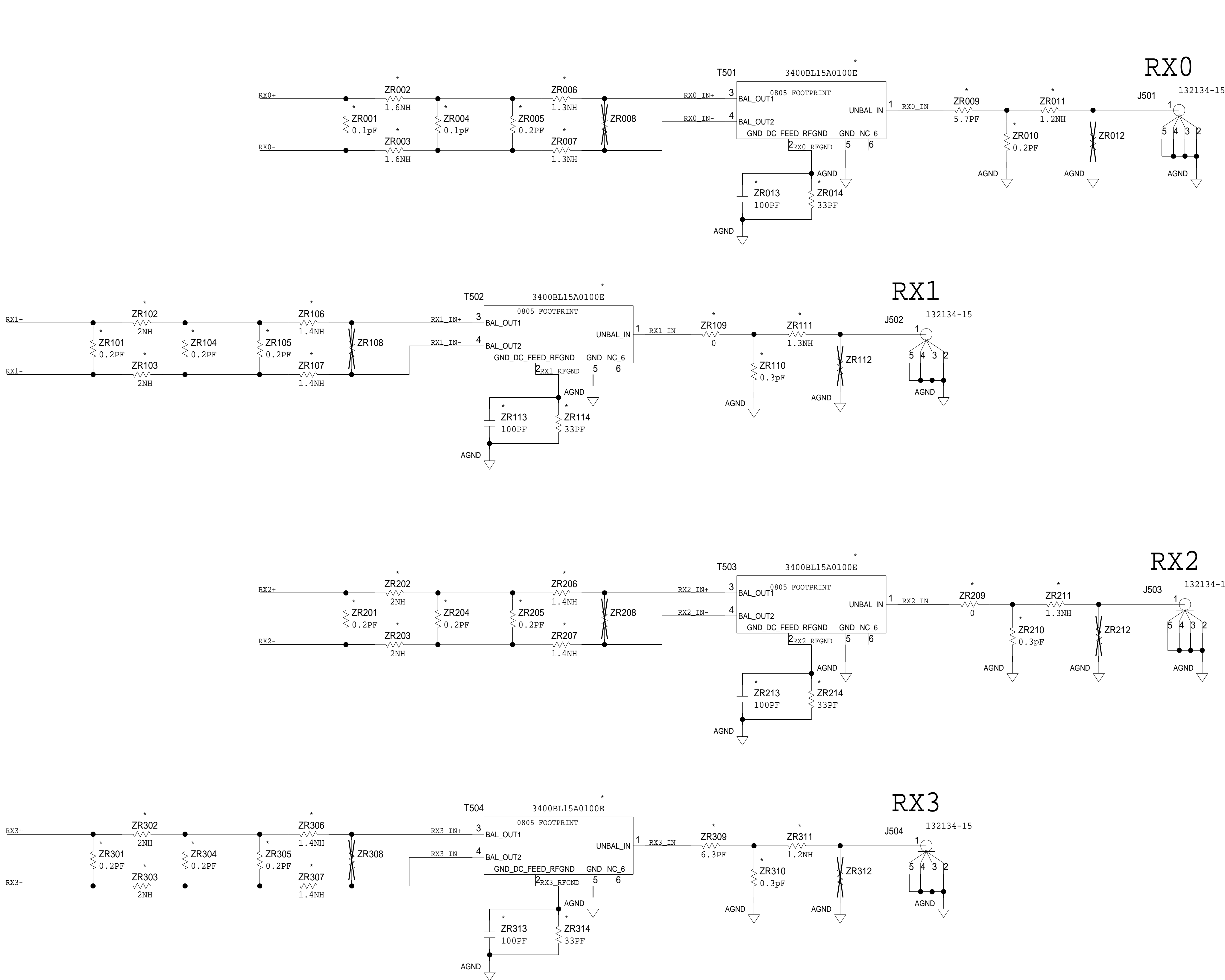


SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 4 OF 19

RECEIVER RF INPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

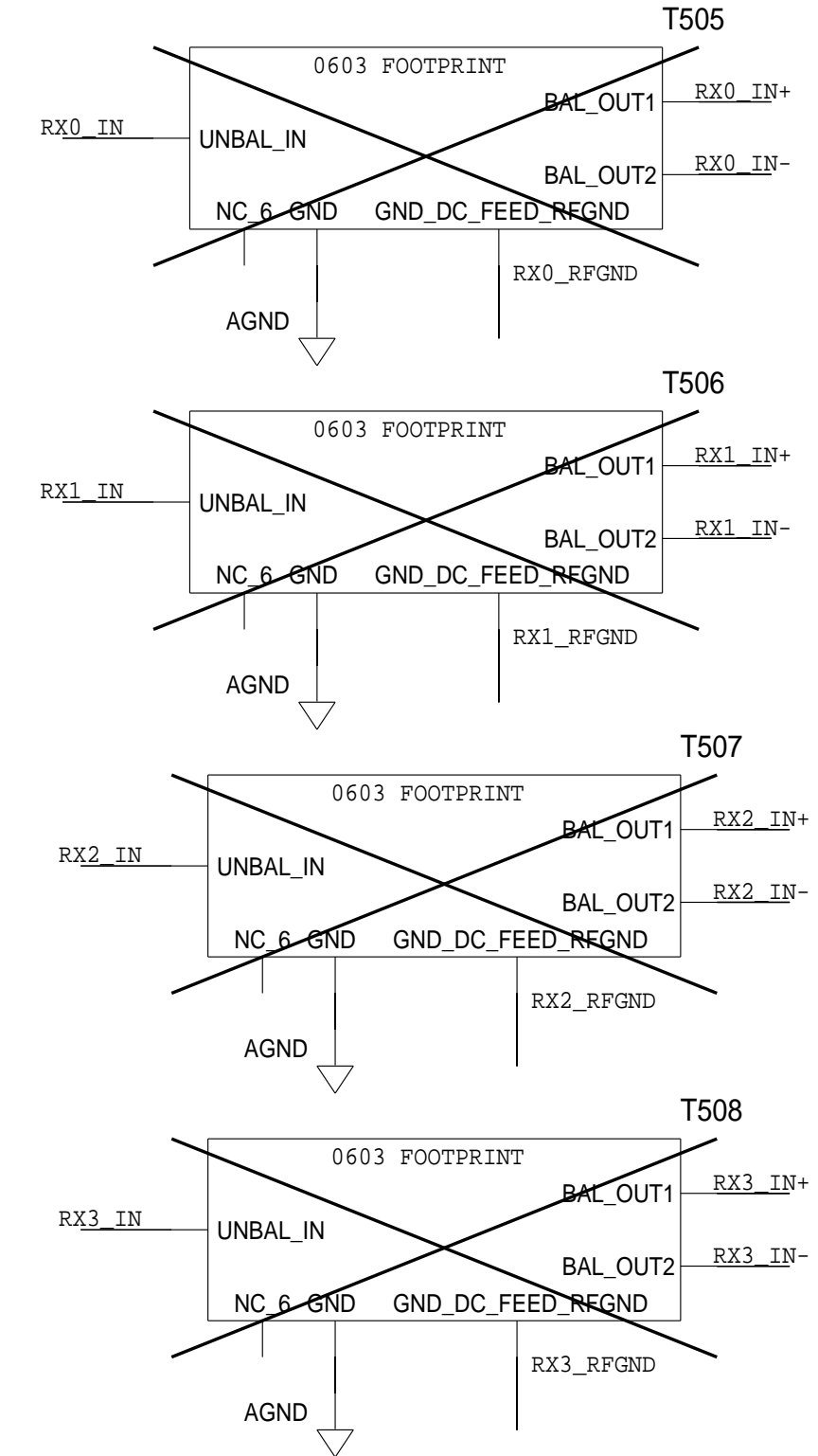
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



U101			
RX0-	D4	RX0N	
RX0+	C4	RX0P	
RX1-	J4	RX1N	
RX1+	H4	RX1P	
RX2-	P4	RX2N	
RX2+	N4	RX2P	
RX3-	W4	RX3N	
RX3+	V4	RX3P	
RX4-	C29	RX4N	
RX4+	D29	RX4P	
RX5-	H29	RX5N	
RX5+	J29	RX5P	
RX6-	N29	RX6N	
RX6+	P29	RX6P	
RX7-	V29	RX7N	
RX7+	W29	RX7P	

ADRV904X-BBCZ

OVERLAP RX BALUNS

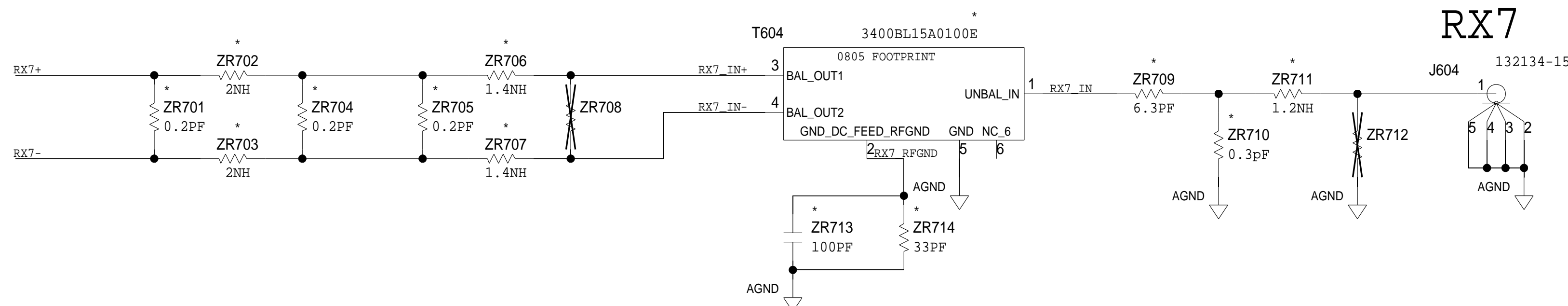
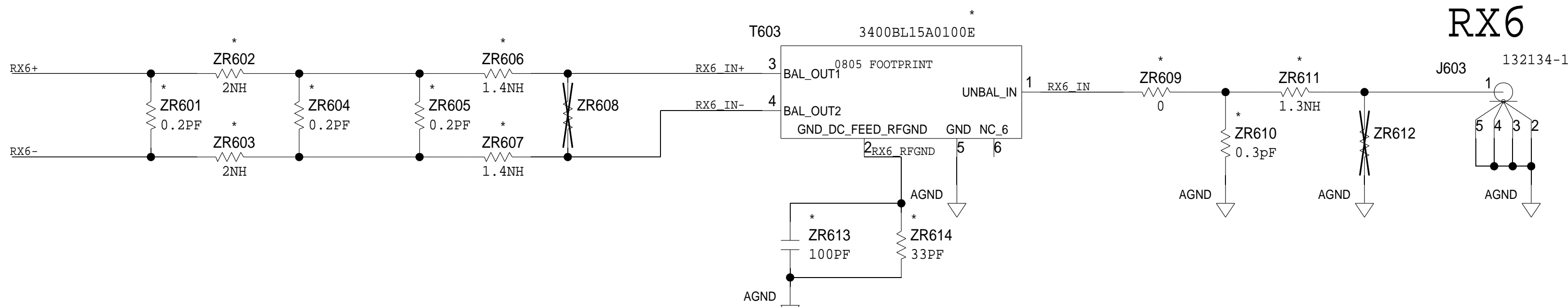
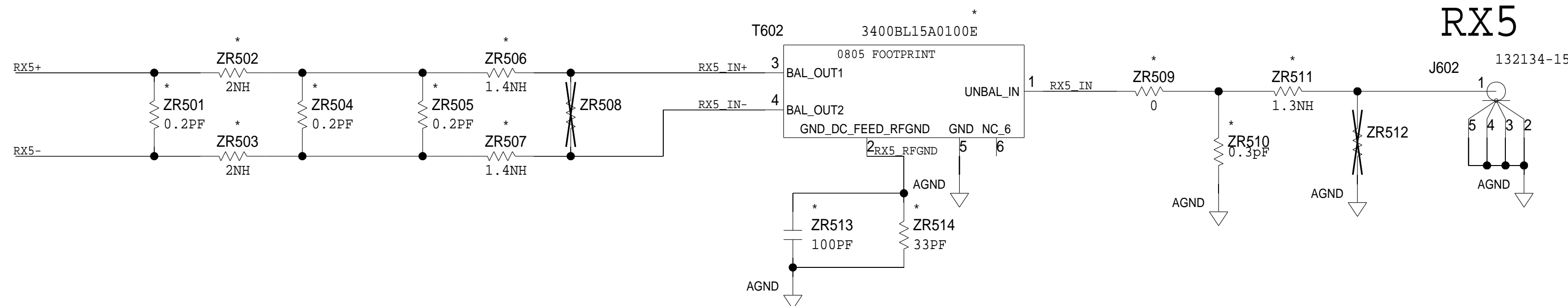
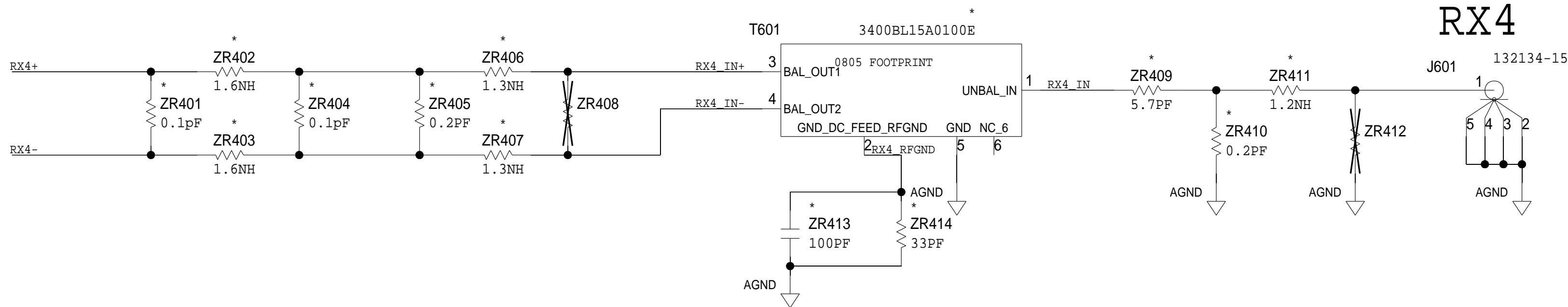


SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 5 OF 19

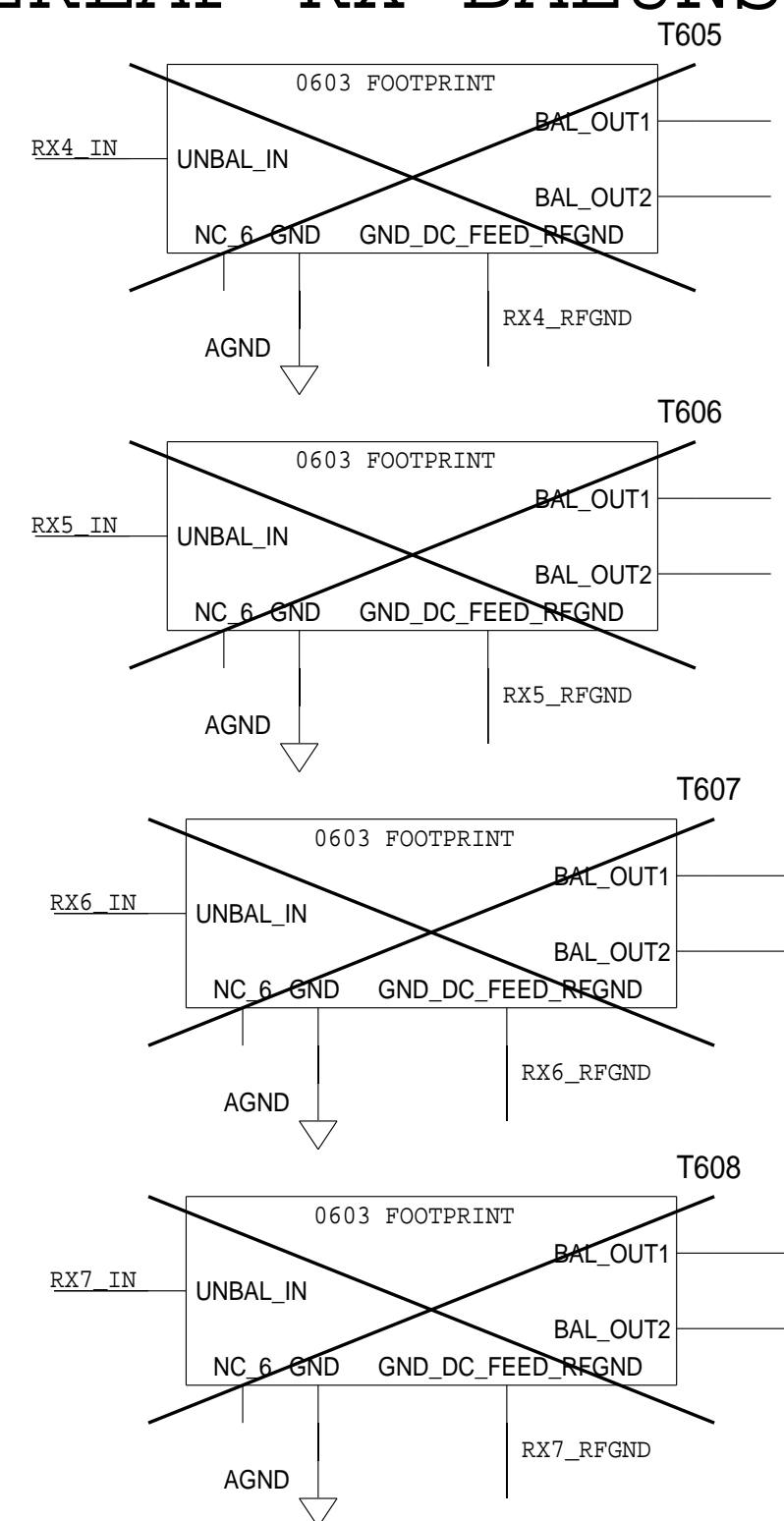
RECEIVER RF INPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



OVERLAP RX BALUNS

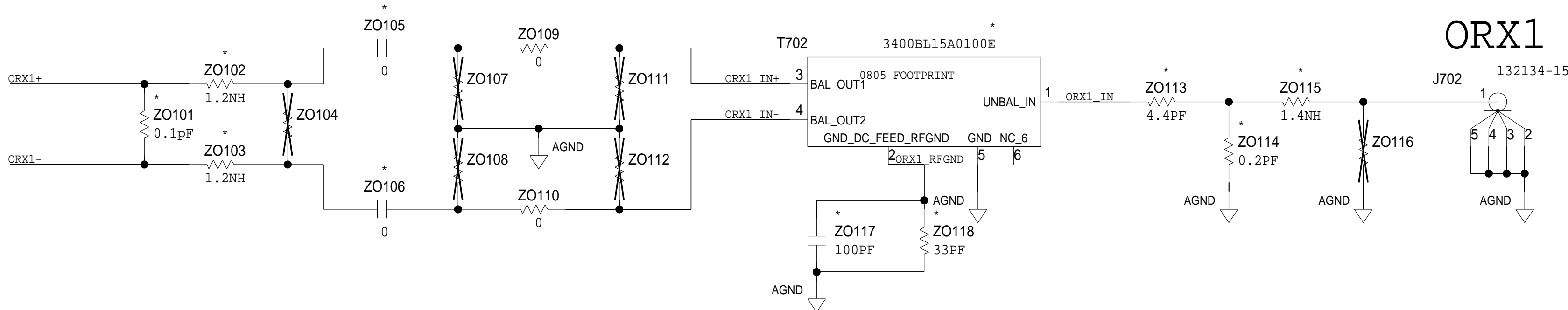
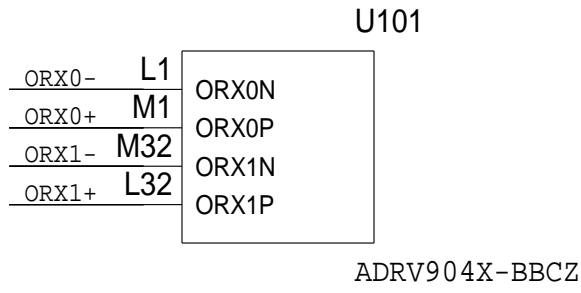
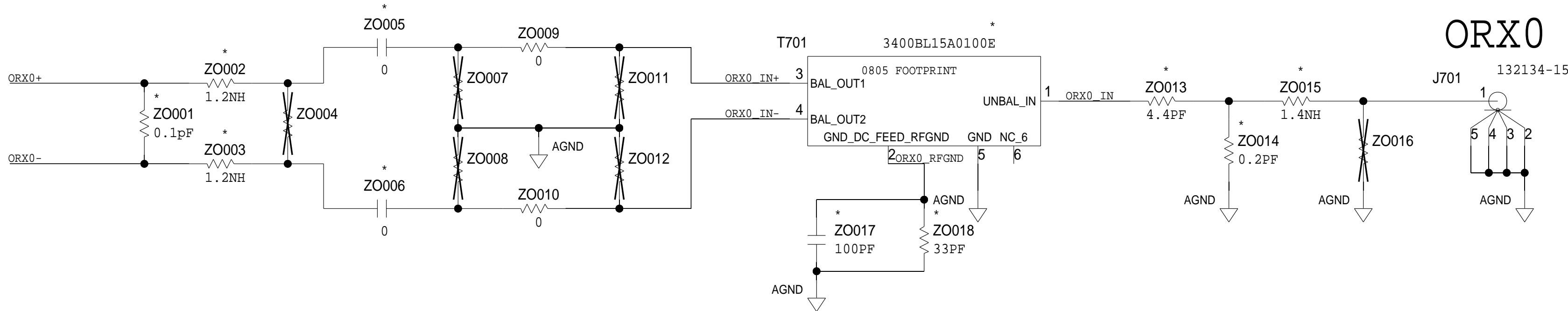


ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795		REV C	
	SIZE D	SCALE 1:1	SHEET 6	OF 19

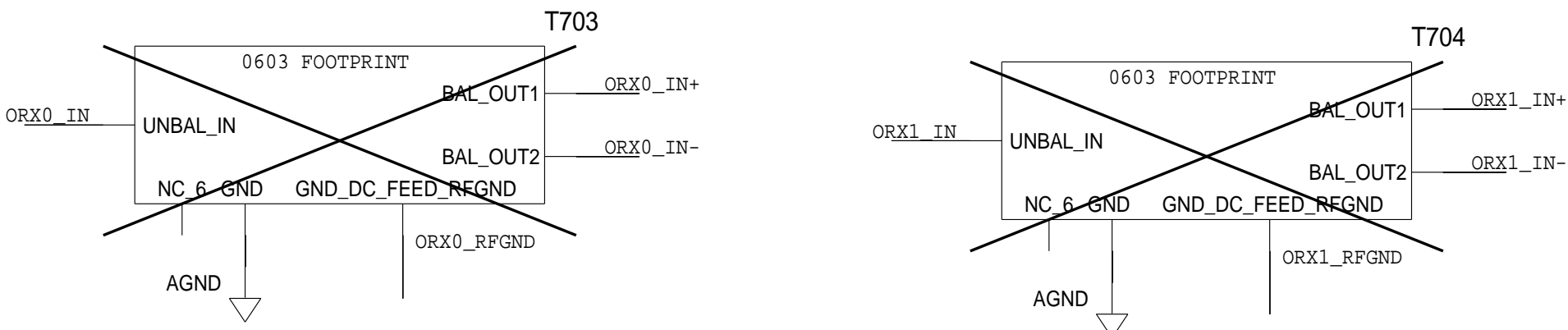
OBSERVATION RX RF INPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



OVERLAP ORX BALUNS



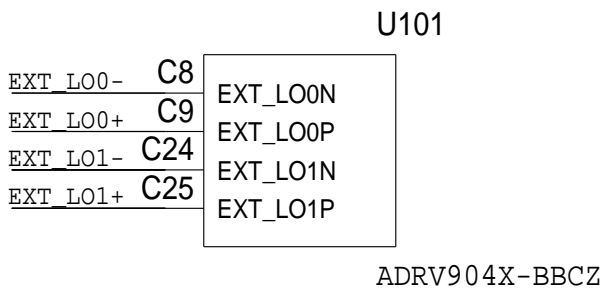
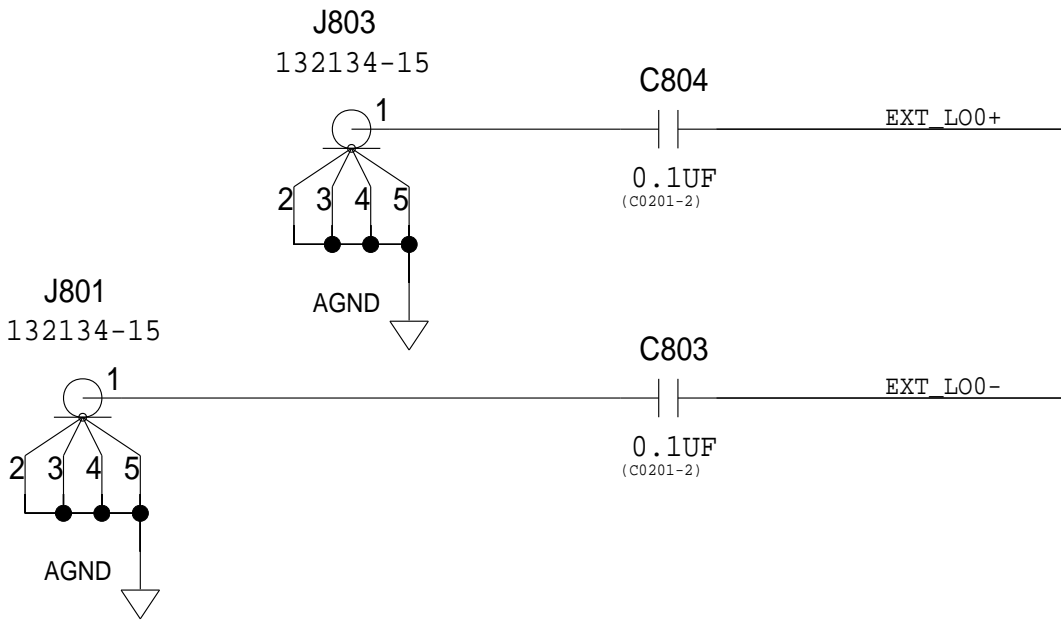
SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 7 OF 19

EXTERNAL LO IN/OUT

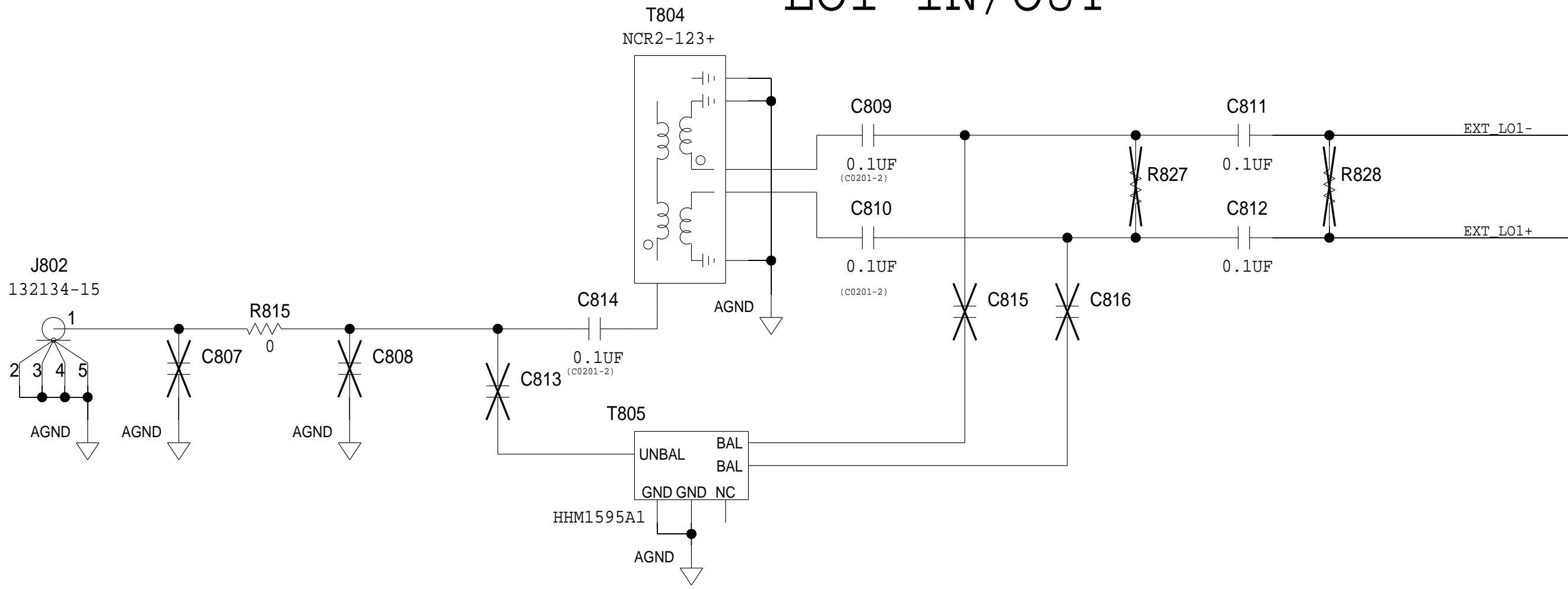
EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

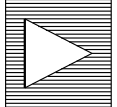
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

LO0 IN/OUT



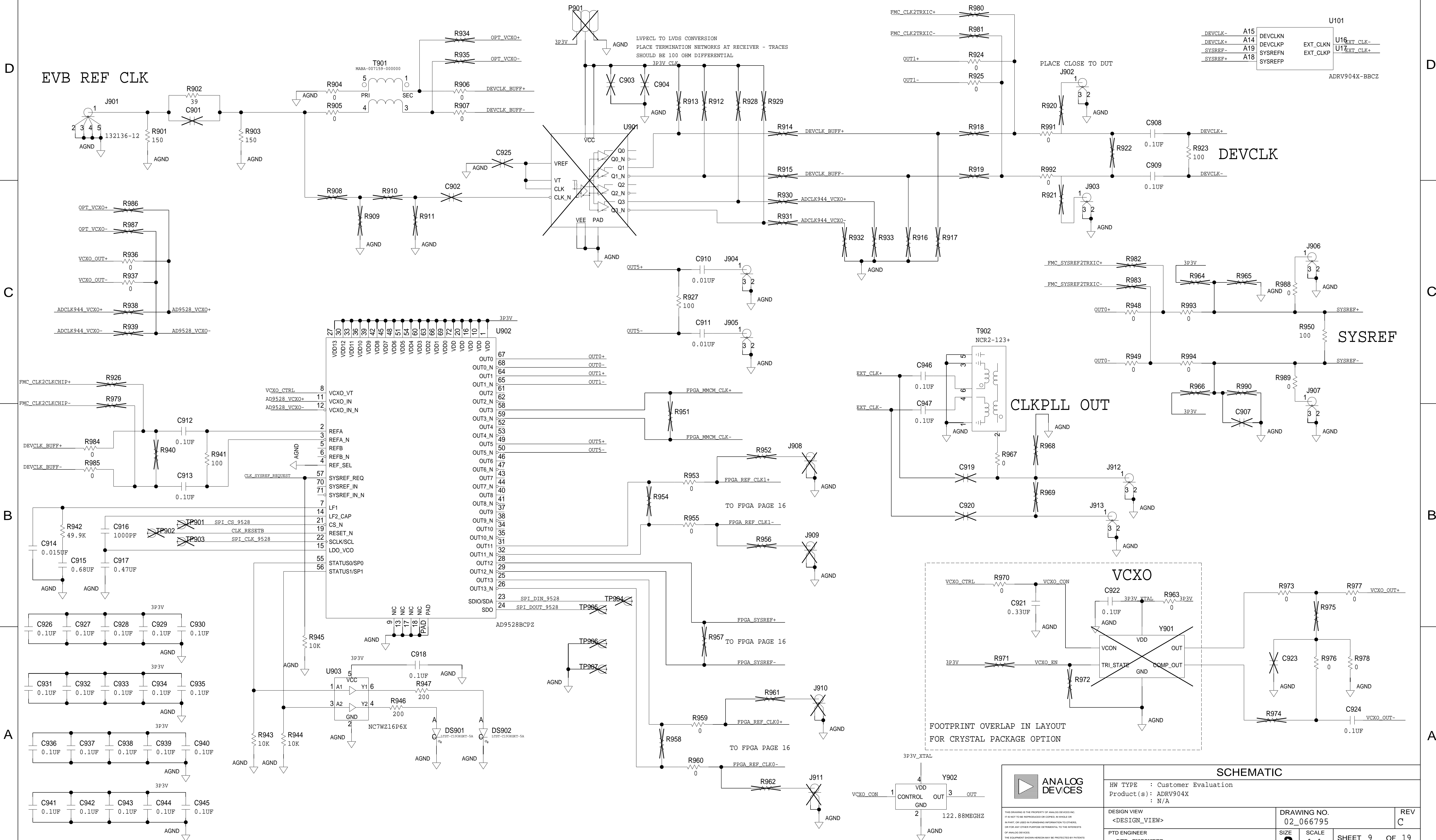
LO1 IN/OUT

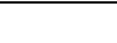


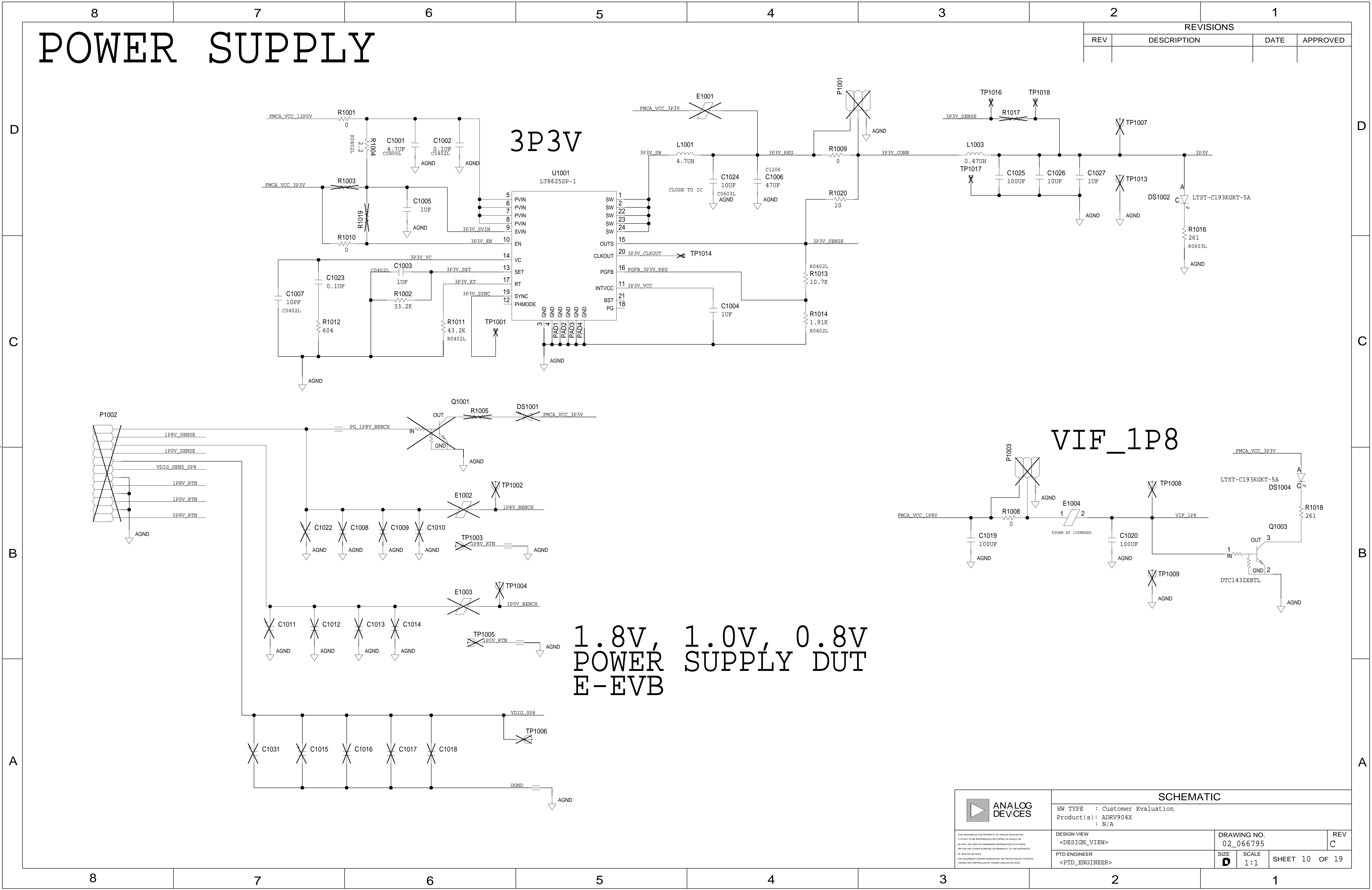
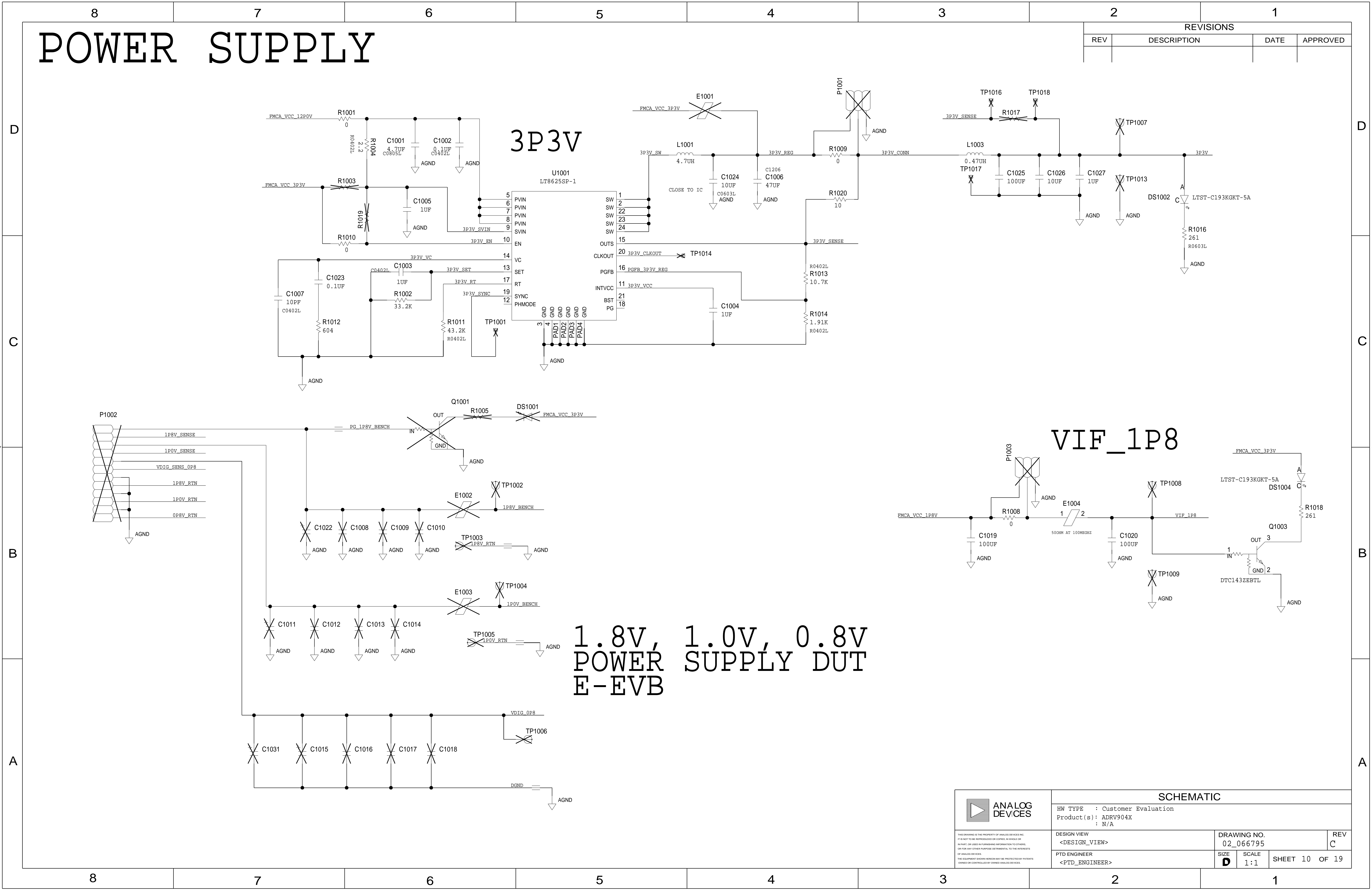
 ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795		REV C
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 8 OF 19

CLOCK GENERATION/DISTRIBUTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	<h1 style="text-align: center;">SCHEMATIC</h1>			
	HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A			
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 9	OF 19

[illegible][illegible]

POWER SUPPLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

3P3V

VIF_1P8

1.8V, POWER E-EVB

1.0V, SUPPLY DUT

0.8V

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s) : ADRV904X : N/A

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
<PTD_ENGINEER>

DRAWING NO.
02_066795

SCALE
1:1

SHEET 10 OF 19

REV C

POWER SUPPLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

3P3V

VIF_1P8

1.8V, POWER E-EVB

1.0V, SUPPLY DUT

0.8V

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s) : ADRV904X : N/A

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
<PTD_ENGINEER>

DRAWING NO.
02_066795

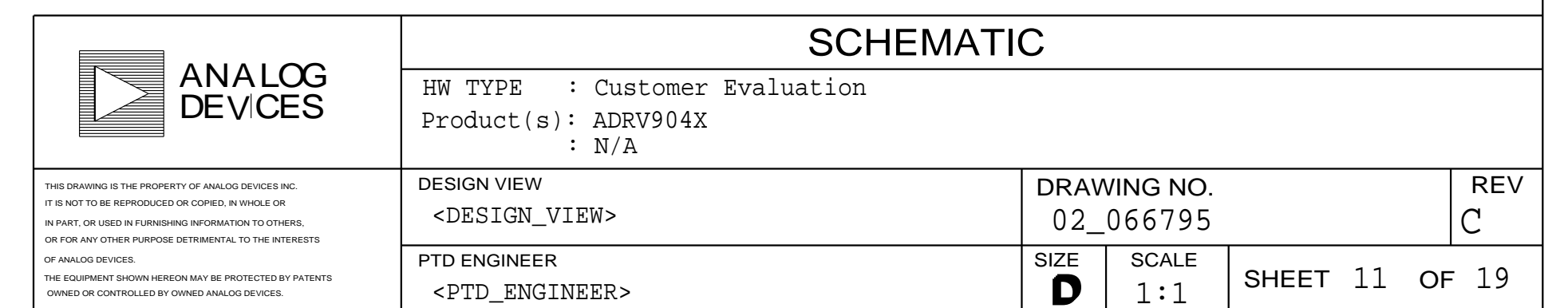
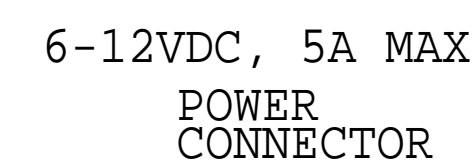
SCALE
1:1

SHEET 10 OF 19

REV C

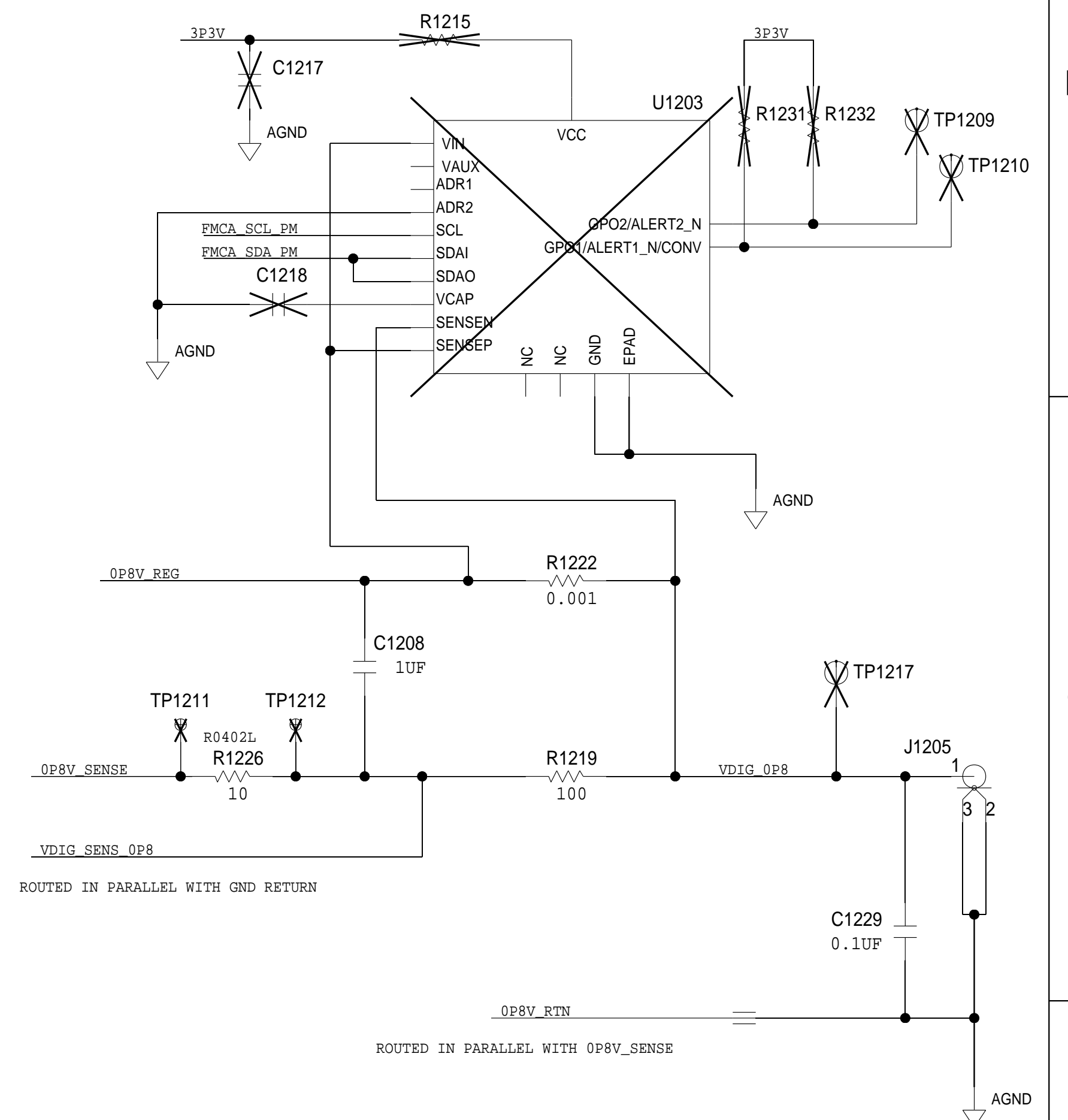
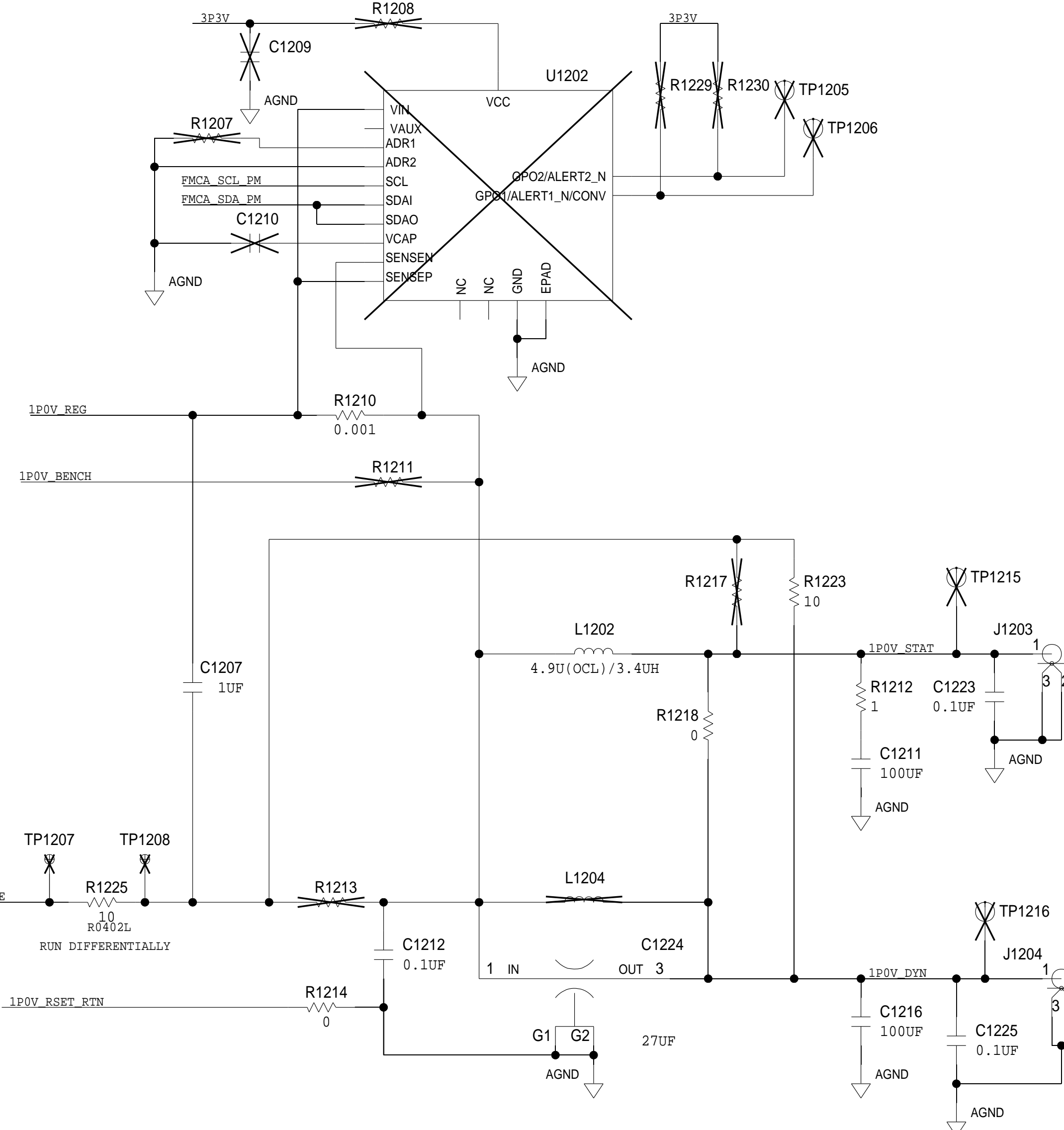
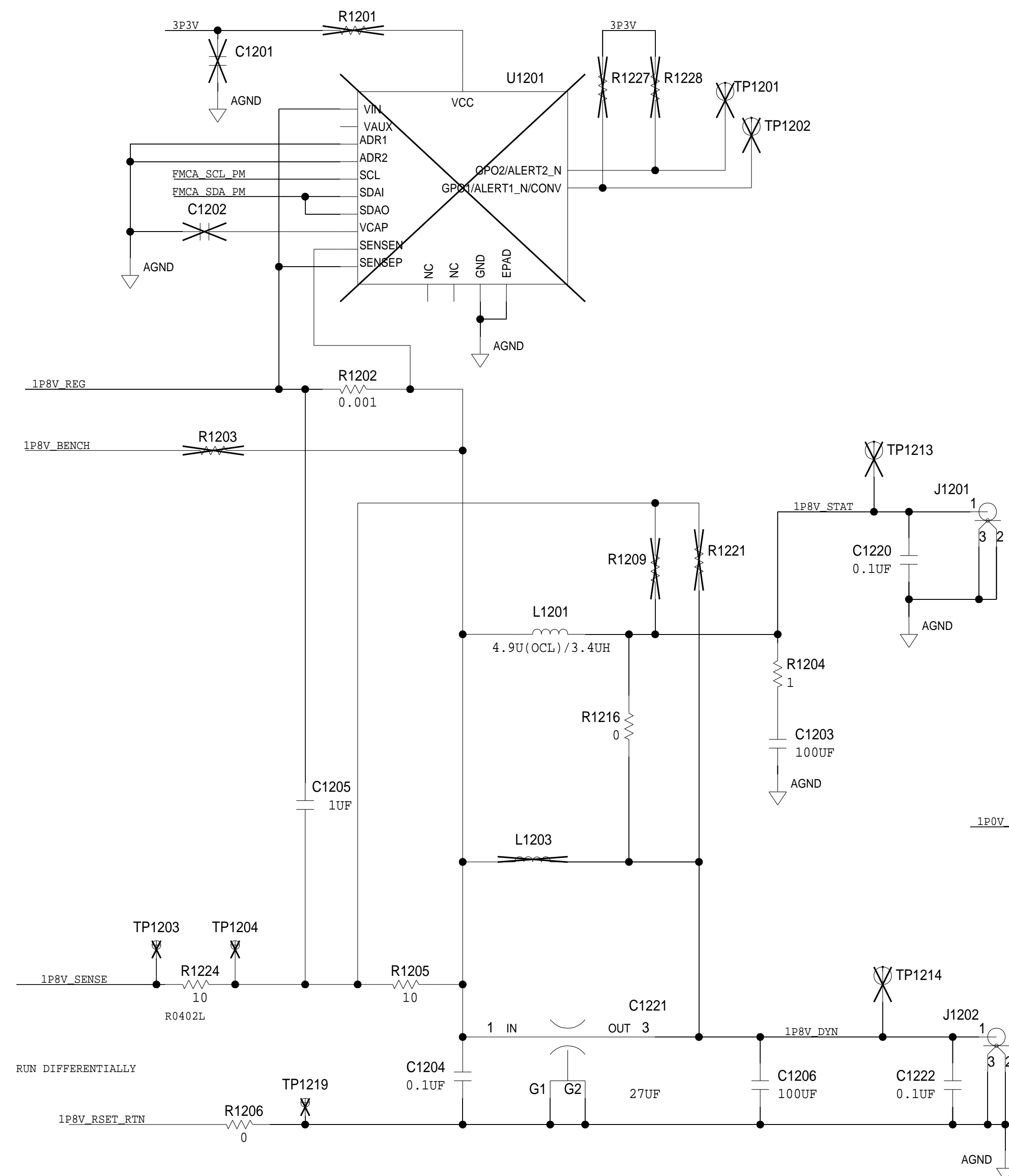
POWER SILENT SWITCHER

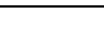
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



POWER MEASUREMENT & FILTERING

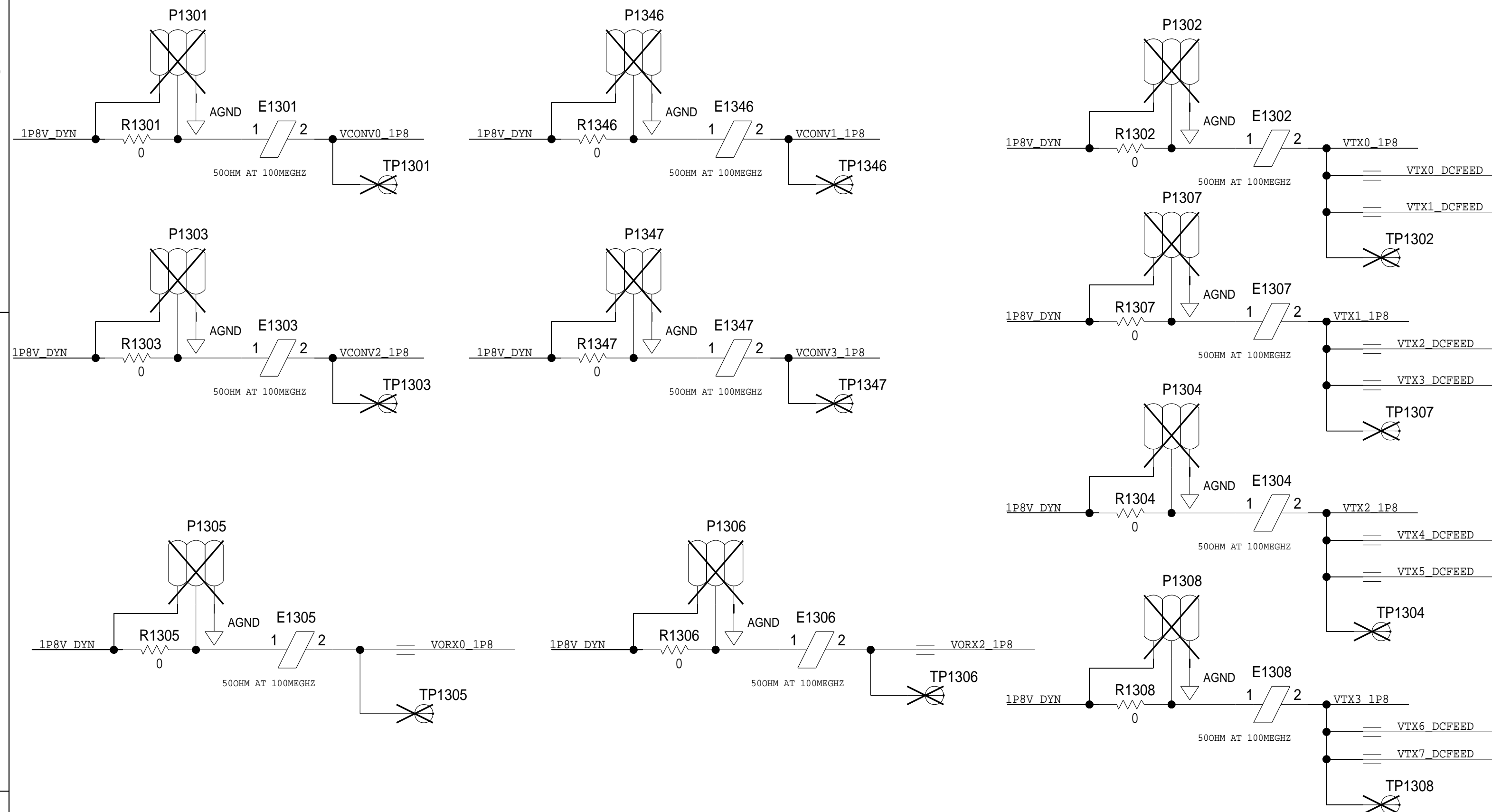
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



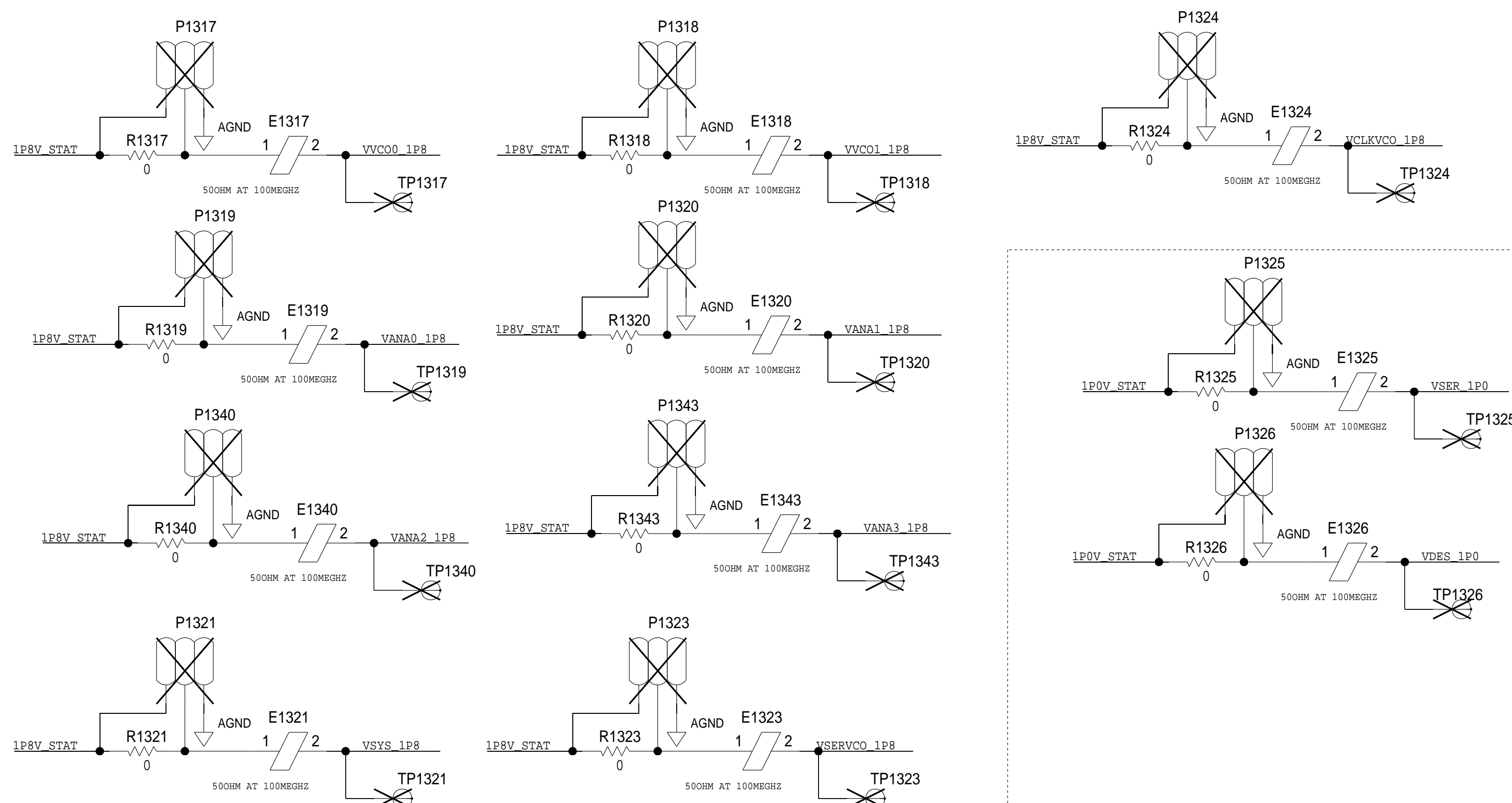
 ANALOG DEVICES		<h1 style="text-align: center;">SCHEMATIC</h1>				
		HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A				
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		PTD ENGINEER <PTD_ENGINEER>		SIZE D	SCALE 1:1	SHEET 12 OF 19

POWER DISTRIBUTION

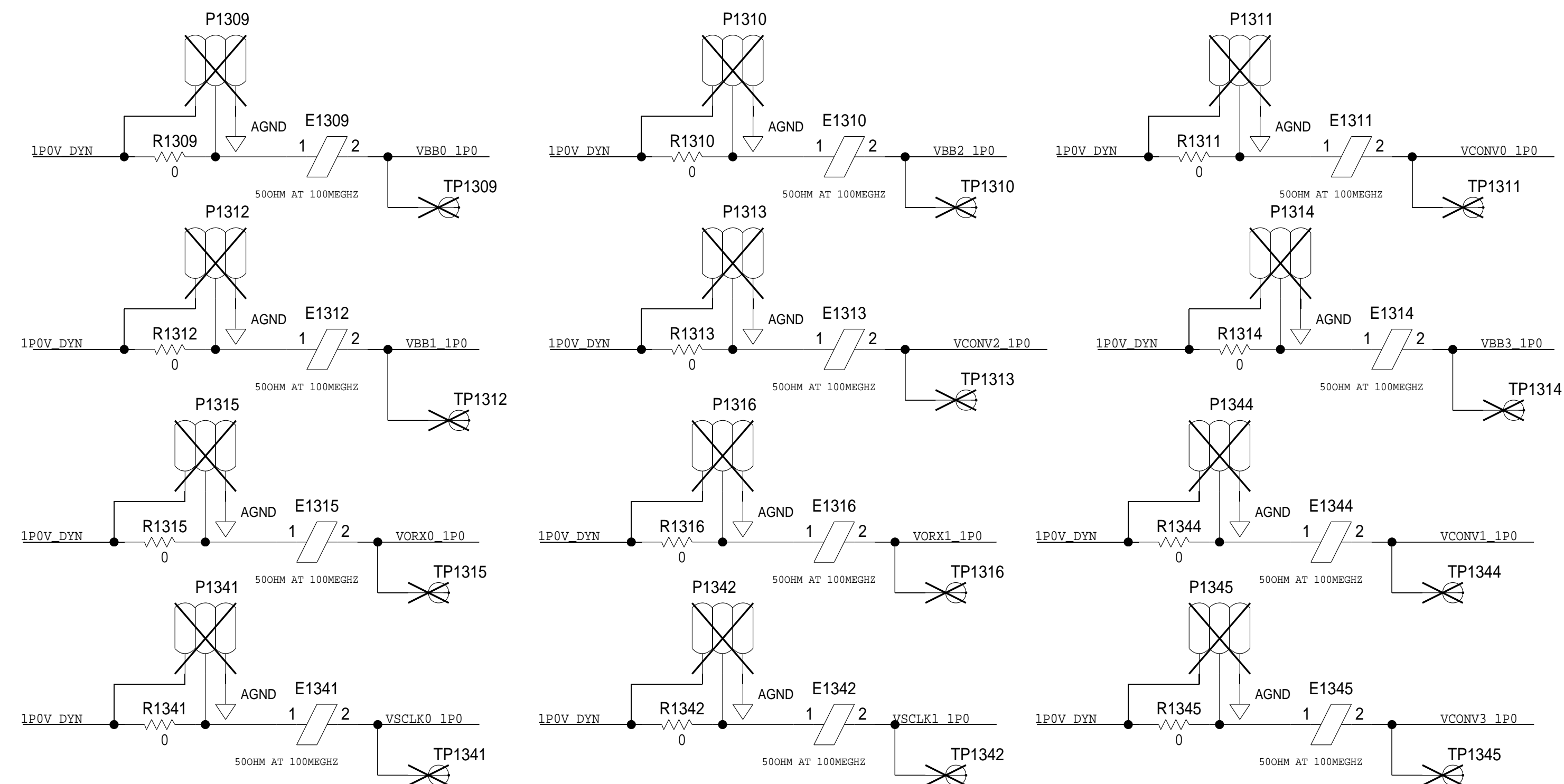
1.8V ANALOG DYNAMIC SUPPLIES



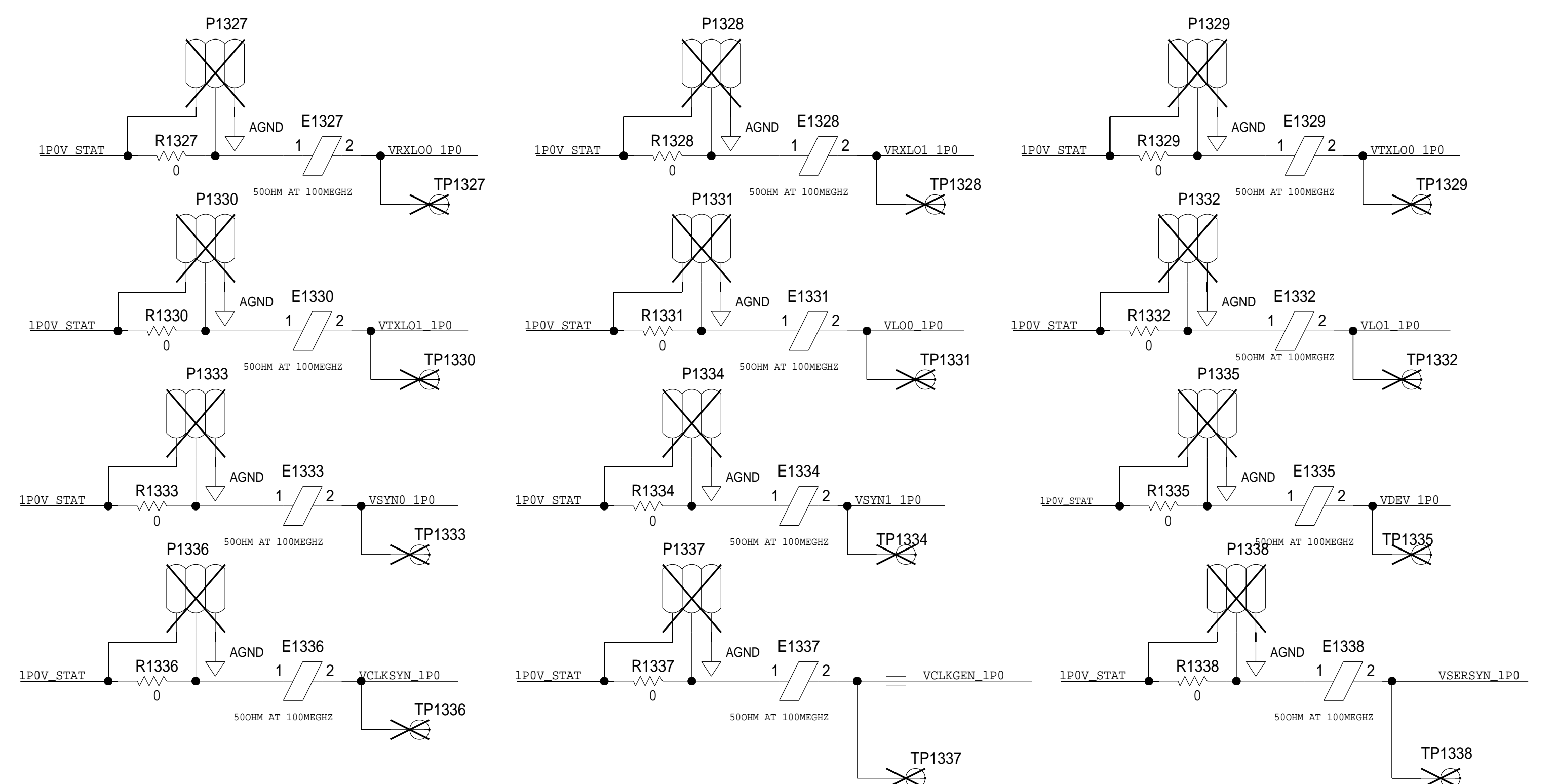
1.8V ANALOG STATIC SUPPLIES

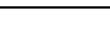


1.0V ANALOG DYNAMIC SUPPLIES



1.0V ANALOG STATIC SUPPLIES



 ANALOG DEVICES	<h1>SCHEMATIC</h1>			
	HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A			
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	PTD ENGINEER <PTD_ENGINEER>		SIZE D	SCALE 1:1
		SHEET 13 OF 19		

POWER INPUT

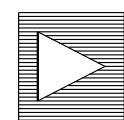
1.8V CAPS

0.8V CAPS

1.0V CAPS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



ANALOG
DEVICES

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SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): ADRV904X
: N/A

DESIGN VIEW

<DESIGN_VIEW>

PTD ENGINEER
<PTD_ENGINEER>

DRAWING NO.

02_066795

REV

C

SIZE

D

SCALE

1:1

SHEET 14

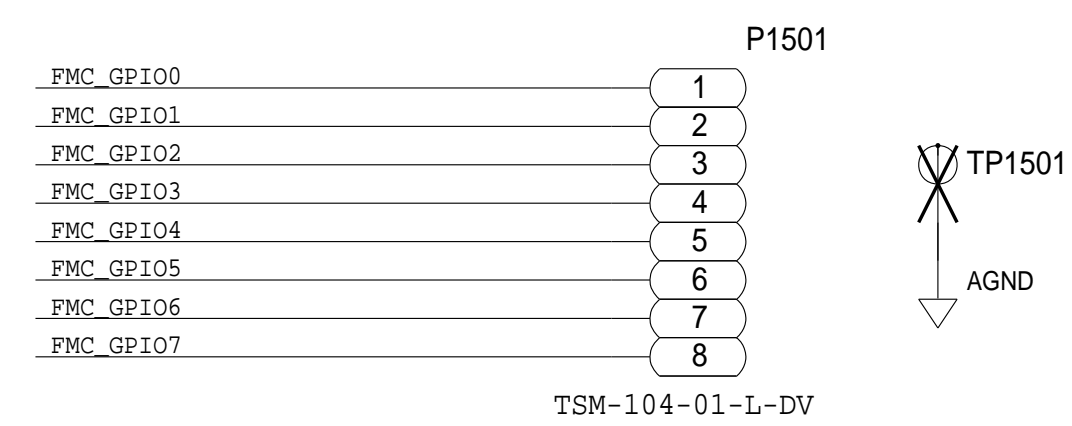
OF 19

ADRV904X-BBC2

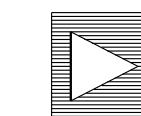
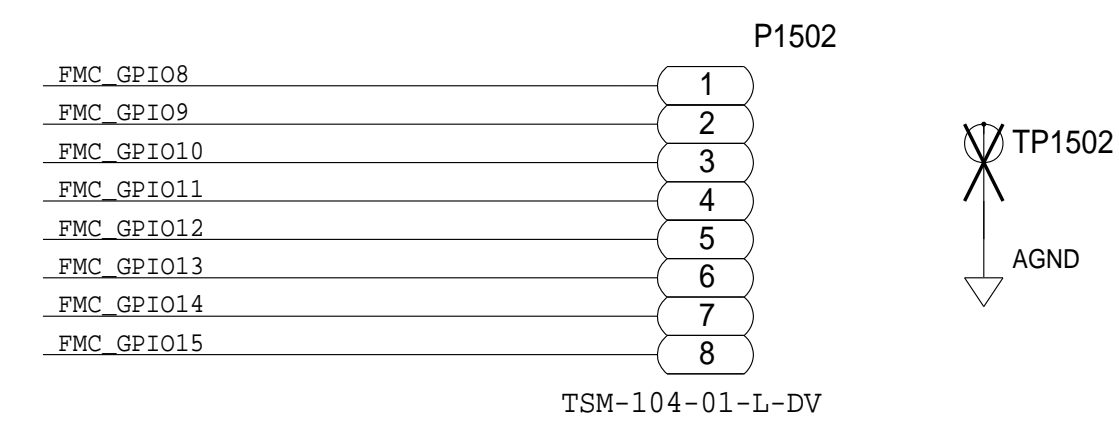
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

RF FRONT END CONTROL INTERFACE

EASTERN 4T4R1ORX



WESTERN 4T4R1ORX



ANALOG
DEVICES

SCHEMATIC

HW TYPE	: Customer Evaluation
Product(s)	: ADRV904X
	: N/A

DESIGN VIEW	
<DESIGN_VIEW>	

DRAWING NO.	02_066795
-------------	-----------

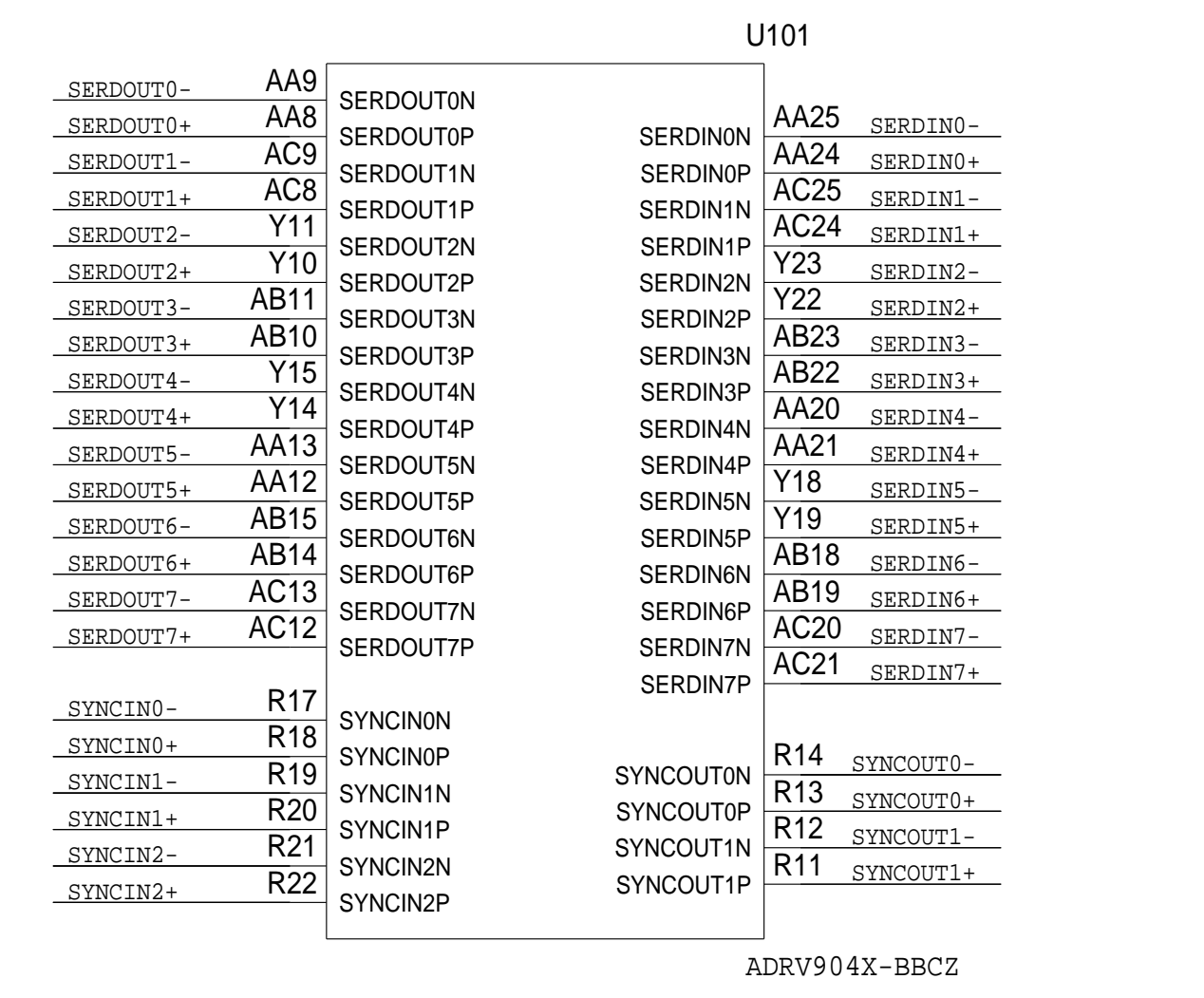
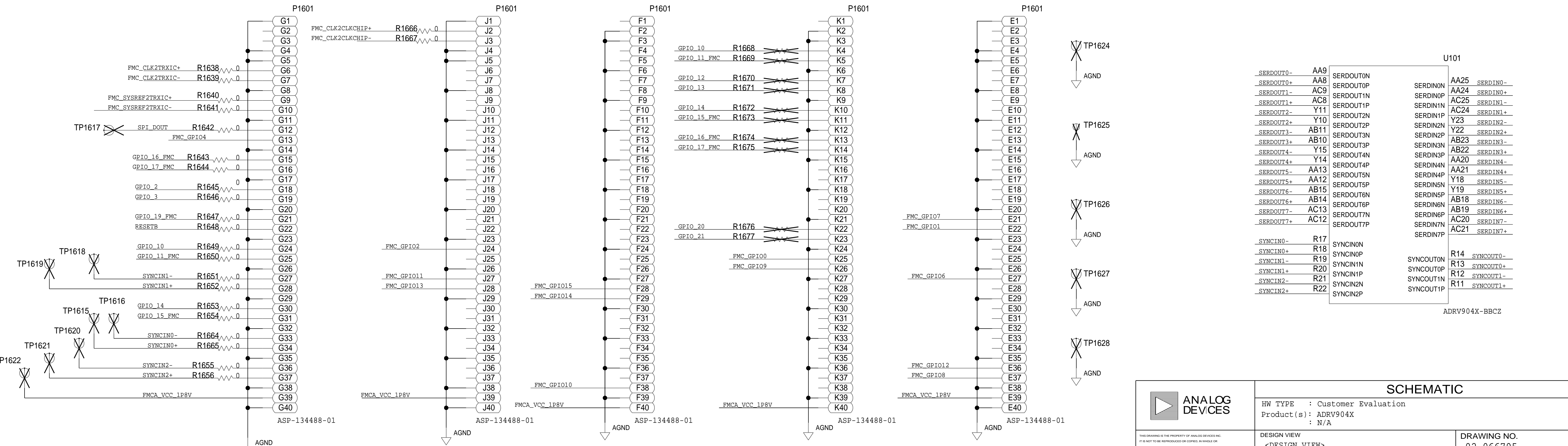
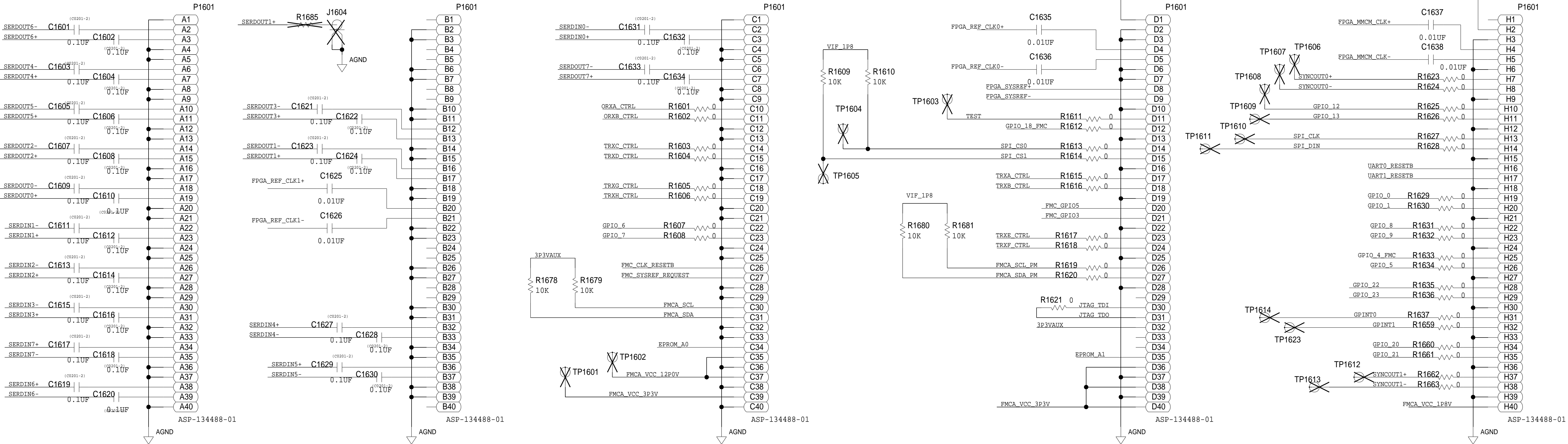
REV	
-----	--

PTD ENGINEER
<PTD_ENGINEER>

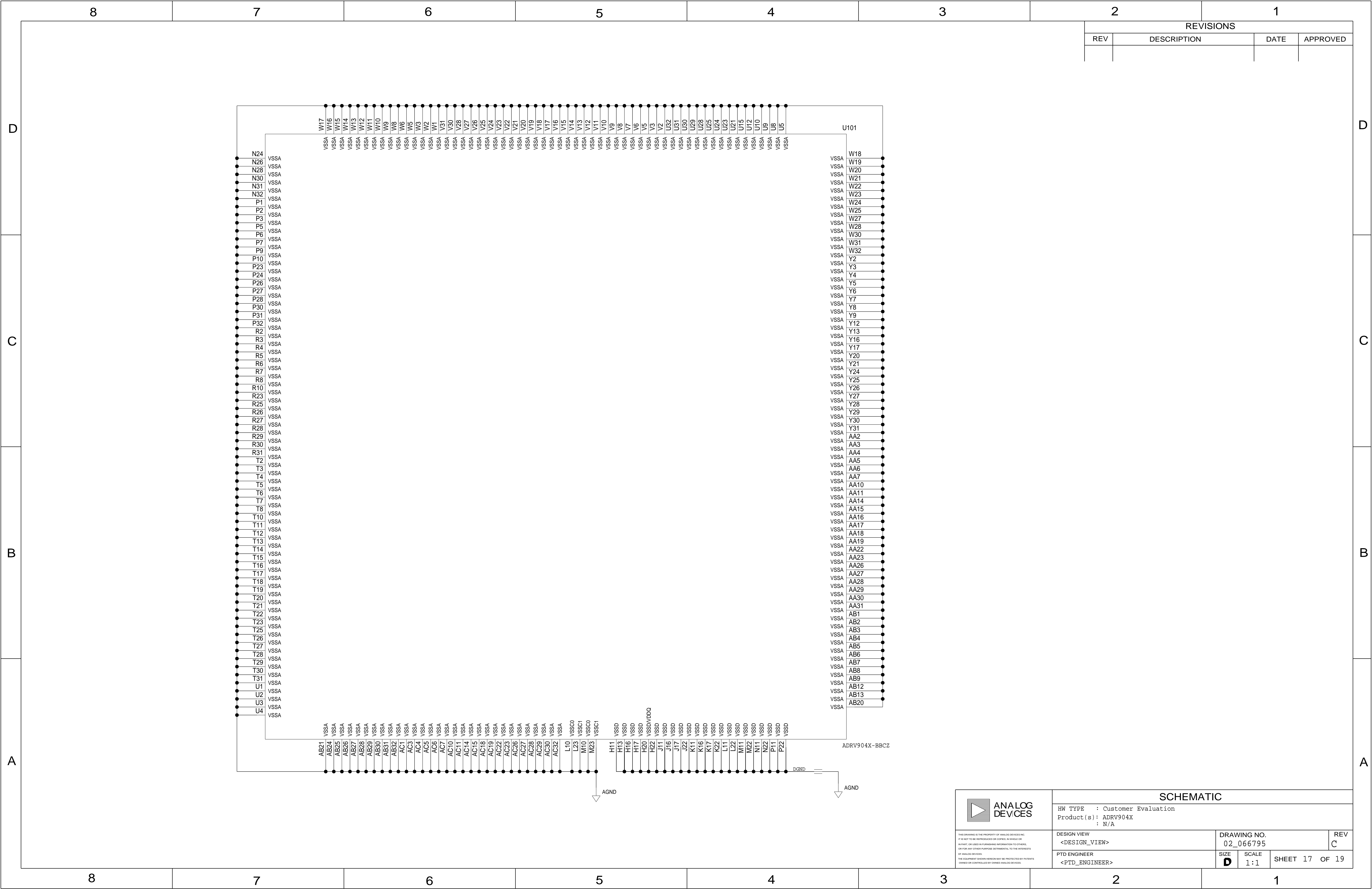
SIZE D	SCALE 1:1	SHEET 15 OF 19
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FPGA CONNECTIONS

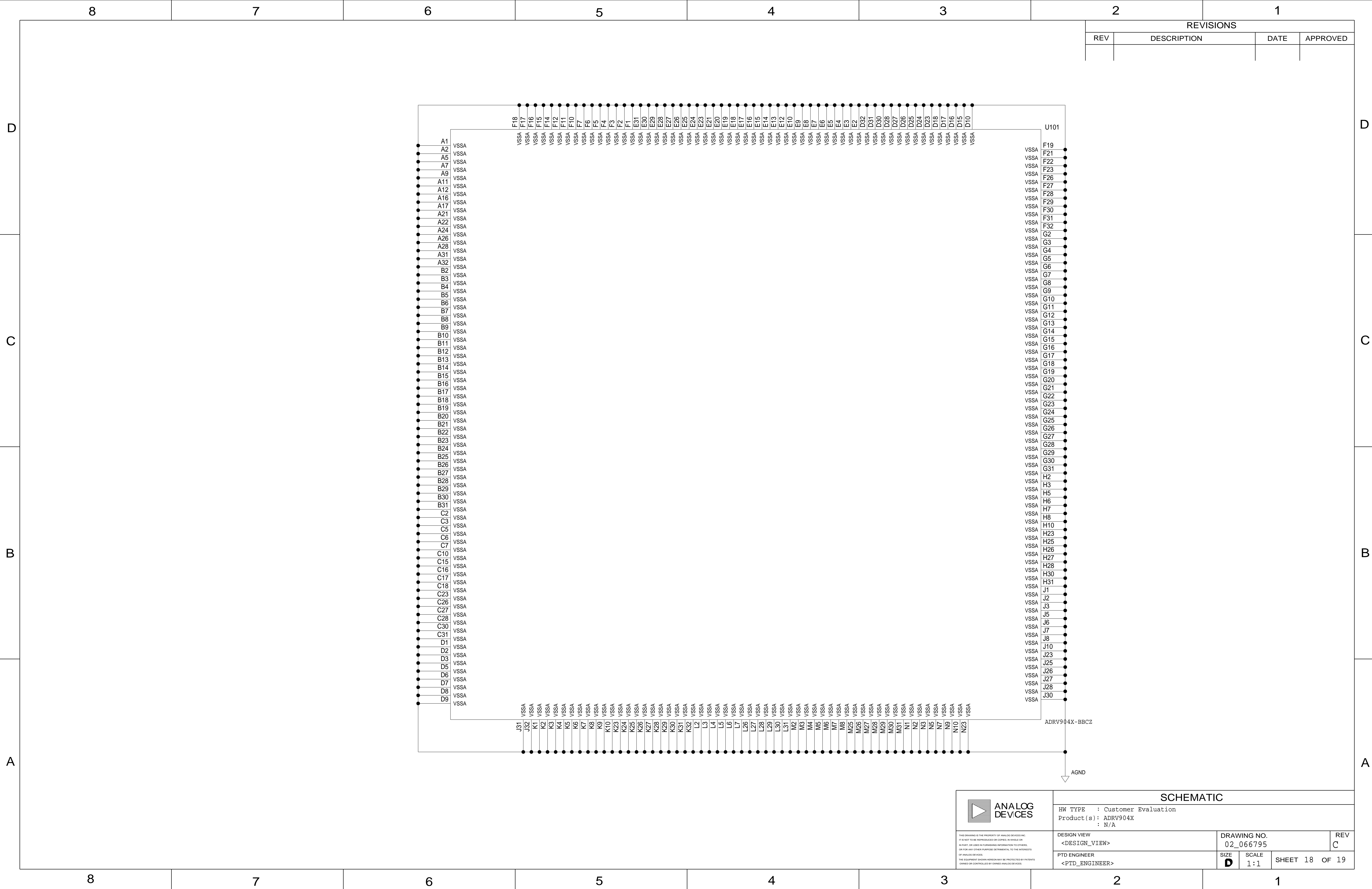
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 16 OF 19



<div><div></div><div>ANALOG DEVICES</div></div>				SCHEMATIC			
HW TYPE : Customer Evaluation				Product(s) : ADRV904X			
				: N/A			
DESIGN VIEW				DRAWING NO.		REV	
<DESIGN_VIEW>				02_066795		C	
PTD ENGINEER				SIZE	SCALE	SHEET 17 OF 19	
<PTD_ENGINEER>				D	1:1		



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
PTD_ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 18 OF 19

